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# An Optimized Grounded Base Oscillator Design for VHF/UHF

*Phase noise in oscillators, along with frequency stability and efficiency, is an important parameter in oscillator design.*

The design of VHF/UHF oscillators has been described in many books and journals with most of the emphasis on frequency stability and to some smaller part on output/efficiency. Since the introduction of reliable phase noise measurements and the ability to predict/simulate the phase noise, the improvement of this important parameter with the help of CAD and analytic equations has gained more attention. The vast majority of early publications focused on designs using small signal approaches, which give non-reliable answers for output frequency, output power and phase noise. The purpose of this paper is to validate the large signal time domain approach using the grounded base oscillator rather than the Colpitts oscillator. The key contributions are: (1) to predict the phase noise correctly using the large signal time domain calculations (Bessel functions) and nonlinear CAD simulators and derive a set of algebraic equations for the noise calculations (many of the CAD tools give incorrect answers about the phase noise), and (2) to provide a set of empirical equations to guide the synthesis of such "optimized" oscillators. This novel design concept using a time domain approach provides both the best output power and the best phase noise.

To have a point of reference the traditional small signal approach is first used followed by the novel approach shown here to get the optimum design. Using a mix of linear equations and one large signal parameter ($g_m$), the important noise parameters are calculated and validated. Finally, based on this, a very simple but powerfully scalable set of formulas for the oscillator synthesis is shown, that provides extremely good results. In addition to this, the design principle for fixed or narrowband oscillator discussed here also applies to the broadband VCO design. We have shown that this design methodology works over a multi-octave tuning range.

## Reference Circuit

A very popular circuit for VHF/UHF oscillators is the grounded base configuration, which is shown in Figure 1. Its phase noise can be made very good, since the RF voltage swing at the collector can be close to the supply voltage. The circuit is simple and has been used for decades. The oscillator function is based on the principle that power from the output is taken and fed to the emitter. This feedback arrangement generates a negative resistance at the output, compensating the losses of the output-tuned circuit, and starts oscillating and then stabilizing the oscillation amplitude[1 – 4]. A

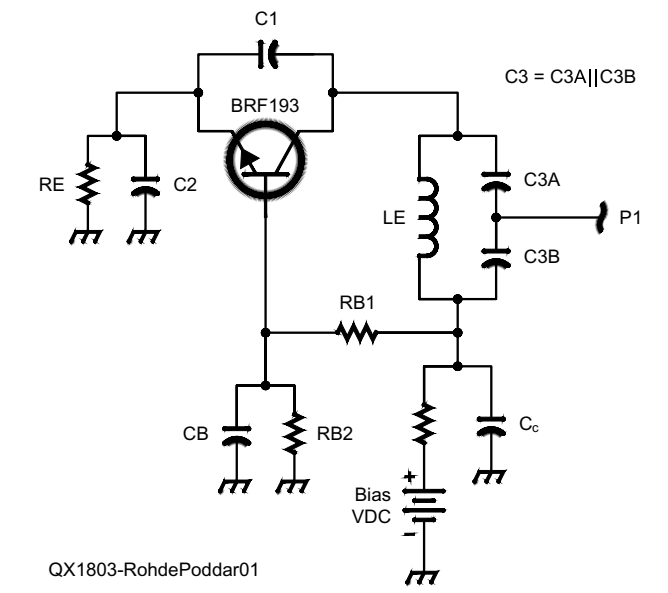


**Figure 1 — Typical configuration of grounded base oscillator circuit.**

complete survey[5 – 19] of configurations and applications is referenced in the Notes. The design methodology works over a 3:1 frequency tuning range[20-23].

Several books on the topic of oscillators have been published in the recent years, and the most popular ones are listed in the Notes. Many of the authors have attempted to predict the oscillator's performance based on a set of linear calculation including using the Leeson model [See Leeson[24]. — *Ed.*] or similar methods to determine the phase noise[25,26]. The problem is that there are important input parameters required, such as the large signal noise figure of the transistor, output power and operating Q. These are typically guessed, but not known. The first successful attempt to determine the large signal phase noise was by Rizzoli, et al.[6] and Annzil, et al.[7].

But these approaches were not useful without a CAD tool and don't give any design guides. Another interesting phenomenon that

has been overlooked by the linear approach is that prediction of the exact oscillator frequency that can be far off compared to the actual frequency of oscillation.

The recent book by Gonzalez[8] gives an interesting overview of designing oscillators using linear calculations and CAD, but his design does not provide the optimum solution. To demonstrate this we are going to first use his way to design a 144 MHz Oscillator. The resulting circuit neither gives the best output power nor the best phase noise and, at high frequencies, requires values for the capacitors, which cannot be easily realized because of parasitic effects. Figure 1 shows the typical configuration of the grounded base oscillator circuit.

This oscillator type works well from RF frequencies like 10 MHz to above 1000 MHz. We will now follow the method of Gonzalez. For large signal conditions see Clarke[11]. Kenneth Clarke was probably the first to publish the effect of the collector current conducting angle of an oscillator, but makes no mentioning of the relationship of it on the phase noise, which is done by Johnson[10].

## The [*Y*] parameters

The first step is to determine the small signal [*Y*] parameters for the transistor BFR 193 (Infineon), at the frequency of 144MHz, and the operating point: $I_c$ = 10 mA, $I_B$ = 24 µA, $V_{be}$ = 0.64V, $V_{ce}$ = 8.8 V

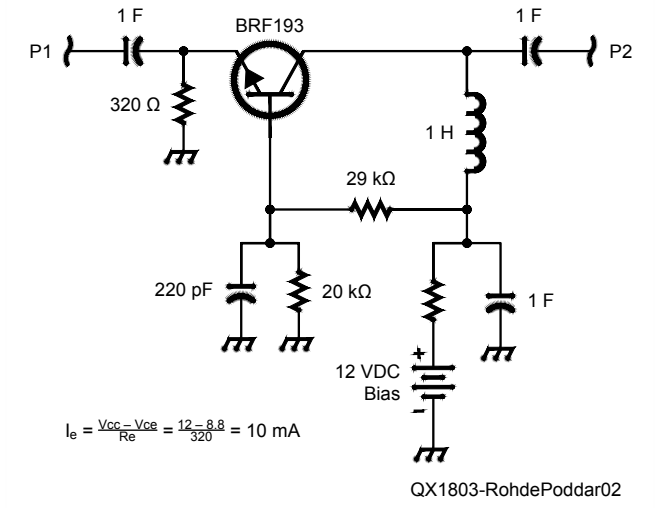


**Figure 2 — Small signal *Y* parameter generating circuit with CAD using Infineon time domain model**

The 10 mA operating point was selected for a stable transistor cut-off frequency $f_T$. For more output power 30 mA is a better choice.

Figure 2 shows the circuit generating the small signal [*Y*] parameters using the Ansoft Designer CAD and the time domain model.

The CAD software generates the *Y*-parameters based on the following definition in Figure 3(a).

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

We obtain:

$$Y_{11} = G_{11} + jB_{11} = (279.08 - j95.07)\ \text{mS}$$
$$Y_{21} = G_{21} + jB_{21} = (-271.32 + j100.77)\ \text{mS}$$
$$Y_{12} = G_{12} + jB_{12} = (-1030 + j78.06)\ \mu\text{S}$$
$$Y_{22} = G_{22} + jB_{22} = (1020 + j536.14)\ \mu\text{S}$$

## Parallel Feedback Oscillator Topology

The feedback arrangement shown in Figure 3(b) is the standard feedback Oscillator topology using parallel elements. Theoretically the grounded base configuration can be rotated to be the Colpitts circuit. This statement is often found in the literature, see Kotzebue and Parrish[5]. It is based on the black box theory. If we look at the performance, it is not correct that a mathematical rotation yields the same performance. In the case of the Colpitts Oscillator the RF voltage swing is now limited by the base emitter and emitter to ground voltage and as a result there is less energy stored in the circuit and because of loading the operational *Q* can be less than in the grounded base configuration. Here $V_{cb}$ is about 12 V. Also $Y_{22cb}$ is less than $Y_{22ce}$, resulting less loading. The Colpitts oscillator is popular because of its simplicity, and its perceived high isolation as the output power is taken at the collector. However, due to the strong Miller effect at very high frequencies, this is not a true statement. These comments set aside the general approach in the time domain shown here is valid not only for the Colpitts Oscillator but other derivatives.

The necessary oscillation condition for the parallel feedback oscillators as shown in Figure 3(b) can be described by

$$Y_{out} + Y_3 \Rightarrow 0$$

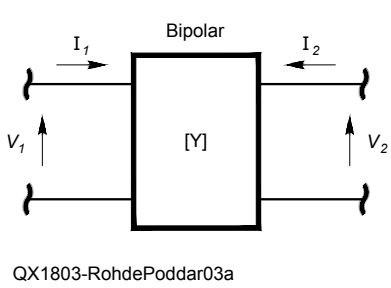


**Figure 3(a) — *Y*-parameters based this definition.**

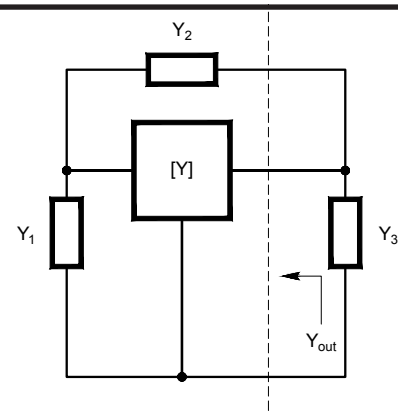


**Figure 3(b) — Parallel feedback oscillator topology.**

This condition can be expressed as

$$Det\begin{bmatrix} Y_{11}+Y_1+Y_2 & Y_{12}-Y_2 \\ Y_{21}-Y_2 & Y_{22}+Y_2+Y_3 \end{bmatrix}=0$$

$$Y_3=-[Y_{22}+Y_2]+\frac{[Y_{12}-Y_2][Y_{21}-Y_2]}{[Y_{11}+Y_1+Y_2]}$$

where $Y_{ij}$ $(i, j = 1, 2)$ are the small signal $[Y]$ parameters of the bipolar or FET model.

**Calculation of the feedback network values [linear case]**

As shown in Figure 3(b), the active 2-port network, together with the feedback elements $Y_1$ and $Y_2$, are considered as a one-port negative resistance oscillator circuit. The following is an example of an oscillator design using the small signal parameter determined above at 8.8 V and 10 mA at 144 MHz. The output admittance $Y_{out}$ is

$$Y_{out}=-Y_3$$

$$\Rightarrow[Y_{22}+Y_2]-\frac{[Y_{12}-Y_2][Y_{21}-Y_2]}{[Y_{11}+Y_1+Y_2]}$$

The optimum values of feedback element are calculated from the expression of $B_1^*$ and $B_2^*$, and for 10 mA are:

$$B_1^*=-\left\{\begin{array}{l} B_{11}+\left[\dfrac{B_{12}+B_{21}}{2}\right] \\ +\left[\dfrac{G_{21}-G_{12}}{B_{21}-B_{12}}\right]\left[\dfrac{G_{12}+G_{21}}{2}+G_{11}\right] \end{array}\right\}$$

$$jB_1^*=j\omega C_1$$

$$C_1\cong 478\,pF$$

$$B_2^*\cong 417\times10^{-3}$$

$$jB_2^*=j\omega C_2$$

$$C_2\cong 459\,pF$$

The optimum values of the real and imaginary part of the output admittance are

$$Y_{out}^*=[G_{out}^*+jB_{out}^*]$$

where

$G_{out}^*$ and $B_{out}^*$ are values for conjugate matching.

$$G_{out}^*=G_{22}-\left[\frac{(G_{12}+G_{21})^2+(B_{21}-B_{12})^2}{4G_{11}}\right]$$

$$\approx -74.5\times10^{-3}$$

needed to compensate the resonator losses ,

$$B_{out}^*=B_{22}+\left[\frac{G_{21}-G_{12}}{B_{21}-B_{12}}\right]\left[\frac{(G_{12}+G_{21})}{2}+G_{22}-G_{out}^*\right]+\left[\frac{B_{21}+B_{12}}{2}\right]$$

$$\approx 214.74\times10^{-3}$$

$$C_3\approx 237\,\text{pF}$$

$$\omega_0=\frac{1}{2\pi\sqrt{LC}};\quad C\approx 471\text{ pF}$$

For $f_0=144$ MHz, $L_3\approx 2.59$ nH

Figure 4 shows the 144MHz oscillator circuit using the small signal $Y$ parameter for establishing oscillation conditions. The required values for this parallel feedback topology are: 478 pF for the feedback capacitor, 459 pF for the emitter to ground, the inductor 3.2 nH, and 186 pF for $C_{3A}$ and $C_{3B}$. The bypass capacitors $C_b$ and $C_c$ should be about 220 pF.

However, it is practically impossible to manufacture capacitors above 200 pF to be capacitive at these frequencies. The best but awkward method then is to use a few capacitors in parallel.

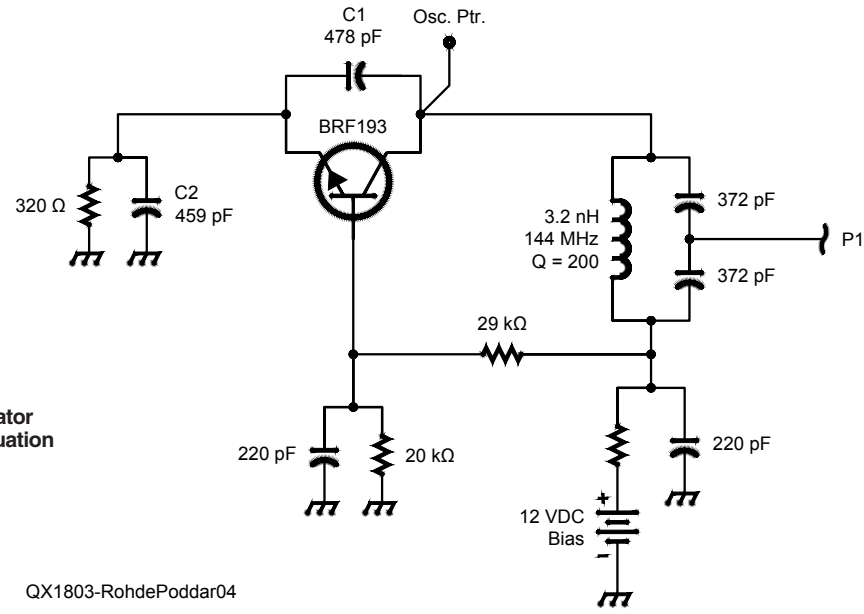


**Figure 4 — 144 MHz oscillator reference circuit for the evaluation of the linear approach.**

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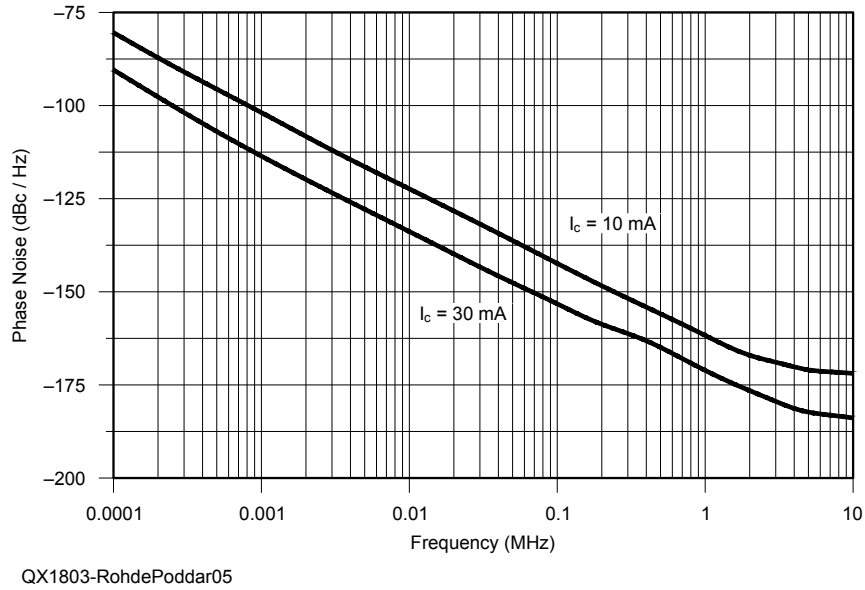


**Figure 5 — Phase noise plot of 144 MHz oscillator reference circuit for the evaluation of the linear approach (both 10 mA and 30 mA cases). The 30 mA case gives 10 dB lower phase noise than the 10 mA case.**

For 30 mA,

$$Y_{11} = G_{11} + jB_{11} = (437 - j295)\ \text{mS}$$

$$Y_{21} = G_{21} + jB_{21} = (-427 + j296)\ \text{mS}$$

$$Y_{12} = G_{12} + jB_{12} = (-1670 + j757)\ \ \mu\text{S}$$

$$Y_{22} = G_{22} + jB_{22} = (1650 - j146)\ \ \mu\text{S}$$

For $f_0$ = 144 MHz and 30 mA, the component values are $L$ = 3.77 nH, $C_1$ = 518 pF, $C_2$ = 503 pF, $C_3$ = 69 pF, $C$ = 324 pF, needless to say $C_1$ and $C_2$ are paralleled capacitors in the vicinity of 100 pF each.

Figure 5 shows the simulated plot of the phase noise. The "linear "calculation indicates a resonant frequency of 143.2 MHz, while the non-linear harmonic balance (HB) analysis supplies the correct frequency of 144.2 MHz (quite a difference in percent) and an output power of just 5.1 dBm, as seen in Figure 6. This value is determined using the HB programs Ansoft Designer (Nexxim). ADS gives the same answer. These CAD tools deviate less then 1 dB from measured results, if the input Spice type parameters for the transistor are accurate.

### Large signal and noise analysis

There were a variety of efforts made to deal with the large signal conditions, like the time domain approach. Equation (10) in Johnson[10] is a first successful attempt to deal with the calculations of the output power with reasonable effort. There are many problems associated with both the large signal analysis as well as the noise analysis. From an experimental point of view it is virtually impossible to build all possible variations. So we were trying to determine if the Ansoft Designer, whose large signal noise analysis development we were involved with, would give us the correct prediction. We were aware that all researchers would primarily look for measured data (which we will show) and yet we had to convince them that our CAD tool

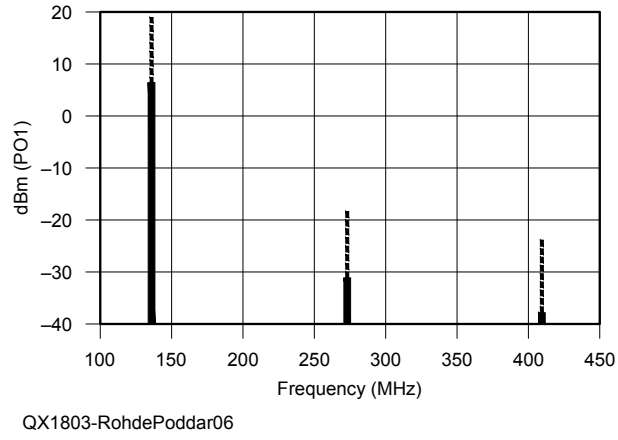


**Figure 6 — RF output power of 144 MHz oscillator reference circuit for the evaluation of the linear approach Both 10 mA (solid) and 30 mA (dashed) are shown. For 30 mA, 12dB more power is available, now a total of approximately 18 dBm.**

was reliable. Therefore we took a few critical circuits, running from crystal oscillators to VCOs and evaluated them again. These were available during the development of the Designer CAD tool, and we re-measured them, with more refined test equipment like the R&S FSUP 26 and its necessary options. We have shown[12, 13] that the accuracy of the prediction was within 0.5 dB of the measured results. During this effort to analyze the noise in oscillators with a set of equations using a minimum of expensive CAD tools, we found this was possible. These equations[9] will be used here.

## A Novel Approach using the time-domain analysis for obtaining the best phase noise and output power.

The hunt for a combined low phase noise can be followed through the literature. Designers have published recipes, like the

use of low noise transistors, high Q circuit, and other things, but the consequences of the large signal operation and the resulting phase noise had not been fully understood. A complete mathematical treatment follows for a 144 MHz oscillator.

**Design steps**

Step 1 — Calculation of the output power for the selected dc operating conditions.

We select the same circuit as above, and set $f_o$ = 144 MHz.

The RF output current is:

$$\begin{aligned} I_{RF}(t) &= I_c(t) \cong I_e(t) \\ &= I_{dc}\left[1+2\sum_{1}^{\infty}\frac{I_n(x)}{I_0(x)}\cos(n\omega t)\right] \\ &= 10\times10^{-3}[1+6.6]_{x=15} \\ &\Rightarrow I_{RF}(t) = 60 \text{ mA peak amplitude} \end{aligned}$$

where $x$ is normalized drive level

$$x = \frac{qV_1}{kT};\ V_1 = \text{Drive signal}$$

Considering 50 Ω load, the RF output power is calculated:

$$\begin{aligned} V_{RF}(f_0) &= I_{RF}\times 50 \\ &= 60\times10^{-3}\times 50 \\ &= 3 \text{ V peak amplitde} \end{aligned}$$

No $V_{ce}$ saturation assumed.

The oscillator output power at 144 MHz is then

$$\begin{aligned} P_{out}(f_0) &= \frac{V_{RF}^2(f_0)}{2R_L} \\ &= \frac{9}{2\times50} = 90 \text{ mW} = 19.5 \text{ dBm} \end{aligned}$$

Step 2 — Calculation of the large signal transconductance for the normalized drive level $x$ = 15

$$\begin{aligned} \cdot Y_{21}\big|_{\text{small signal}} &= \frac{I_{dc}}{kT/q} = \frac{I_{dc}}{V_T} = g_m \\ \Rightarrow g_m &= \frac{3\times10^{-3}}{26 \text{ mV}} \approx 115 \text{ mS} \end{aligned}$$

where $k$ is the Boltzman constant, and $T$ = 298 K.

The large signal transconductance $G_m$ is now

$$\begin{aligned} Y_{21}\big|_{\text{large-signal}} &= G_m(x) = \frac{qI_{dc}}{kTx}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \\ &= \frac{g_m}{x}\left[\frac{2I_1(x)}{I_0(x)}\right]_{n=1} \\ &\approx 20 \text{ mS (for } x \approx 15) \end{aligned}$$

This assumes an ideal intrinsic transistor. To perform the transition from the intrinsic to extrinsic transistor, we add the parasitics (package effects, lead inductance and bond wires) by correcting the final results for capacitances and inductances. The $f_t$ of the transistor used is high enough so a phase shift correction for $g_m$ is not necessary at this frequencies (VHF).

The value of $n$ can be in the range of $n$ [$n_1$, $n_2$], where $n_1$ is 2 and $n_2$ is 5 for a drive level $x$ = 15 (low phase noise performance).

Assume $n$ = 5, the values of $C_1$ and $C_2$ can be calculated to be

$$\frac{C_2}{C_1+C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{4} \Rightarrow \frac{C_1}{C_2} = 4$$

The ratio of the capacitor $C_1$ to $C_2$ is 4.

Step 3 — Calculation of $C_1$ and $C_2$.

The value of $C_1$ is selected for proper loading, therefore

$$\begin{aligned} &XC_1 > Y_{11} \approx C_1 > \frac{Y_{11}}{\omega} \\ &\Rightarrow C_1 > \frac{Y_{21}}{\omega} \cong C_1 \geq \frac{2G_m(x)}{\omega} \\ &\Rightarrow C_1 > \frac{2\times20\times10^{-3}}{2\times\pi\times144\times10^6} \approx 44 \text{ pF} \end{aligned}$$

For $C_1/C_2$ = 4, $C_2 \cong$ 11 pF.

Step 4 — Calculation of $C_3$ and $C_4$.

For optimum phase noise and power output,

$$C_3 \geq 2C_2 \Rightarrow C_3 = 22 \text{ pF},$$

and the capacitive transformer tapping ratio $m$ ($C_3/C_4$) should be greater than 10, therefore the impedance transformation is greater than 100. For $C_3$ =22 pF, $C_4$ is 220 pF.

Step 5 — Calculation of $L$.

$$\omega_0 = \frac{1}{2\pi\sqrt{LC}};$$

$$C = C_T + C_3;$$

$$C_T = \frac{C_1\times C_2}{C_1+C_2} \Rightarrow C \approx 30 \text{ pF}$$

For $f_0$ = 144 MHz,

$$L_3 = \frac{1}{(2\pi\times144\times10^6)^2\times29\times10^{-12}} \approx 39 \text{ nH}$$

Step 6 — Calculation of the [$L/C$] ratio.

The energy stored across the resonator circuit for a given conduction angle and drive level is dependent on the characteristic impedance,

$$Z_0 = \sqrt{\frac{L(\text{nH})}{C(\text{pF})}} = \sqrt{1200}$$

For optimum phase noise and output power, $Z$ should be greater than 3.

For example, the $L/C$ ratio for a good approach is

$$\frac{L_3}{C_3} = \frac{39\times10^{-9}}{30\times10^{-10}} = 13 \Rightarrow p > 10$$

Validation — We now use the same test circuit and apply the "new" component values just calculated.

### Phase Noise Calculation

We have shown[9] the phase noise calculations for the Colpitts oscillator. These calculations can also be used to get the phase noise of this circuit. It agrees well with both measurements and simulations using the harmonic balance simulator Ansoft Designer (Nexxim).

The individual phase noise contribution can be described by

$$PN_{inr}(\omega_0+\Delta\omega) = \frac{4KT}{R_P}\left[NFT_{inr}(\omega_0)\right]^2$$

$$= \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2j\omega_0 C_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

→ Phase noise contribution from the resonator tank.

$$PN_{Vbn}(\omega_0+\Delta\omega) = 4KTr_b\left[NFT_{Vbn}(\omega_0)\right]^2$$

$$= 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2jQ}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

→ Phase noise contribution from the base resistance.

$$PN_{ibn}(\omega_0+\Delta\omega) = 2qI_b\left[NFT_{ibn}(\omega_0)\right]^2$$

$$= 2qI_b\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{j\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

→ Phase noise contribution from the base current.

$$PN_{ifn}(\omega_0+\Delta\omega) = \frac{K_f I_b^{AF}}{f_m}\left[NF_{ibn}(\omega_0)\right]^2$$

$$= \frac{K_f I_b^{AF}}{f_m}\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{j2\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

→ Phase noise contribution from the flicker noise of the transistor.

$$PN_{icn}(\omega_0+\Delta\omega) = 2qI_c\left[NFT_{icn}(\omega_0)\right]^2$$

$$= 2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2j\omega_0 QC_{eff}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$

→ Phase noise contribution from the collector current.

The total effect of all the four noise sources can be expressed as

$$PN(\omega_0+\Delta\omega) = [PN_{inr}(\omega_0+\omega)] + [PN_{Vbn}(\omega_0+\omega)] + [PN_{ibn}(\omega_0+\omega)] + [PN_{icn}(\omega_0+\omega)]$$

where

$K_f$ = Flicker noise constant

$AF$ = Flicker noise exponent.

$$C_{eff} = C + \frac{C_1C_2}{C_1+C_2}$$

Note that the effect of the loading of the Q of the resonator is calculated by the noise transfer function multiplied with the noise sources.

The phase noise contribution from the different noise sources for the parallel tuned Colpitts oscillator circuit at $\Delta f$ = 10 kHz from the oscillator frequency $f_0$ = 144 MHz will now be computed.

### Circuit parameters

Base resistance of transistor $r_b$ = 6.14 Ω.
Parallel loss resistance of the resonator $R_P$ = 7056 Ω.
Q of the resonator = 200 (Q of the inductor at 144 MHz)
Resonator inductance = 39 nH
Resonator capacitance = 22 F
Collector current of the transistor $I_c$ = 10 mA
Base current of the transistor $I_b$ = 85 μA.
Flicker noise exponent $AF$ = 2
Flicker noise constant $K_f = 10^{-7}$
Feedback factor $n$ = 5.
Phase noise at 10 kHz is
$PN_{inr}(\omega_0 + 10\text{ kHz}) \approx -134.2$ dBc/Hz
$PN_{Vbn}(\omega_0 + 10\text{ kHz}) \approx -151$ dBc/Hz
$PN_{(ibn+ifn)}(\omega_0 + 10\text{ kHz}) \approx -169.6$ dBc/Hz
$PN_{icn}(\omega_0 + 10\text{ kHz}) \approx -150.6$ dBc/Hz

The total sum of all the four noise sources can be expressed as

$$PN(\omega_0+\Delta\omega) = [PN_{inr}(\omega_0+\omega)] + [PN_{Vbn}(\omega_0+\omega)] + [PN_{ibn}(\omega_0+\omega)] + [PN_{icn}(\omega_0+\omega)] \cong -134.1 \text{ dBc/Hz}$$

Note that the noise contribution from the resonator at this offset is the same as the flicker noise contribution from the transistor. For low-Q cases, this can be identified as the flicker corner frequency.

Phase noise at 100 Hz is
$PN_{inr}(\omega_0 + 100\text{ Hz}) \approx -94.2$ dBc/Hz
$PN_{Vbn}(\omega_0 + 100\text{ Hz}) \approx -111$ dBc/Hz
$PN_{(ibn+ifn)}(\omega_0 + 100\text{ Hz}) \approx -124.1$ dBc/Hz
$PN_{icn}(\omega_0 + 100\text{ Hz}) \approx -110.6$ dBc/Hz

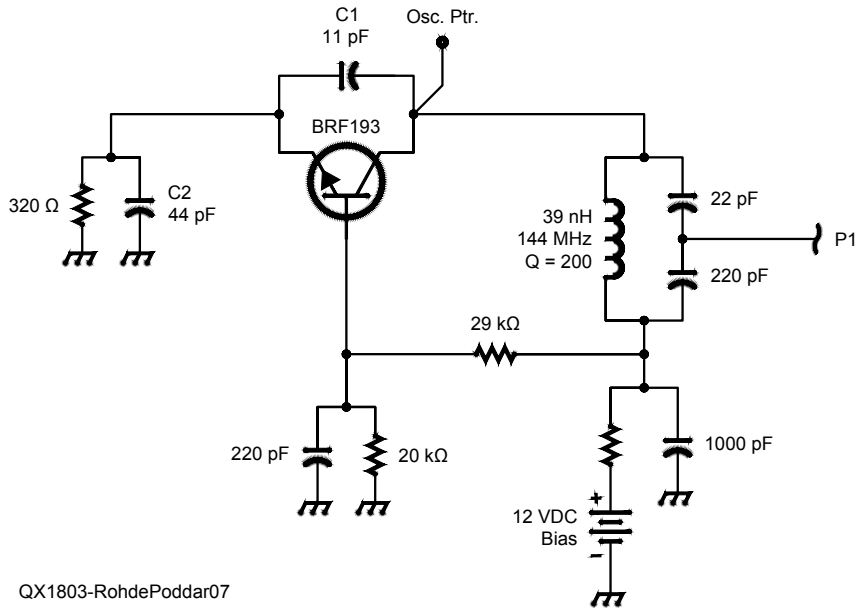


**Figure 7 — 144 MHz oscillator reference circuit for the evaluation of the time domain approach.**

The total sum of all the four noise sources can be expressed as

$$\begin{aligned} PN(\omega_0+\Delta\omega) &= [PN_{inr}(\omega_0+\omega)] \\ &\quad +[PN_{Vbn}(\omega_0+\omega)] \\ &\quad +[PN_{ibn}(\omega_0+\omega)] \\ &\quad +[PN_{icn}(\omega_0+\omega)] \\ &\cong -94.1\,\text{dBc/Hz} \end{aligned}$$

It appears that the flicker noise and the noise from the resonator are the limiting factors for the overall phase noise performance of the oscillator circuit.

Figure 7 shows the schematic and Figure 8 shows the layout of the 144 MHz oscillator using time domain parameters at $I_c$ = 10 mA. The oscillator circuit shown in Figure 7 uses a lumped inductor of 39 nH and an unloaded Q of 200 at the operating frequency. Even at these frequency the layout is quite critical. The Figure 8 layout shows an assembly of component where the lead inductances have been kept small. The inductor is a standard off the shelf component.

Figures 9 shows the CAD simulated phase noise plot, and Figure 10 shows the measured phase noise plot. The simulated and the validated output power now is 11.55 dBm (a 6 dB improvement compared to the linear case), and at 10 kHz offset from the carrier frequency the phase noise has been improved to be –135 dBc/Hz from previously –122 dBc/Hz, a 13 dB improvement. The outputs at the second and third harmonics are about -28 dBm and -34 dBm.

Using our phase noise calculation approach as shown above, the result is –134 dBc/Hz and –94 dBc/Hz at 10 kHz and 100 Hz offset. All three results, calculated, simulated, and measured result closely agrees within 1 dB. Many designers may not have access to CAD tools with oscillator noise calculation, and therefore this approach is extremely useful and cost saving.

If we now operate the same transistor at 30 mA, the phase noise at 10 kHz offset will be further improved to –144 dBc/Hz and the output power is increased to 20 dBm. This shows that for low phase noise design a more powerful transistor is a good choice. It is important to keep the dc dissipation of the device in mind, as the CAD approach does not flag a misuse of the device.

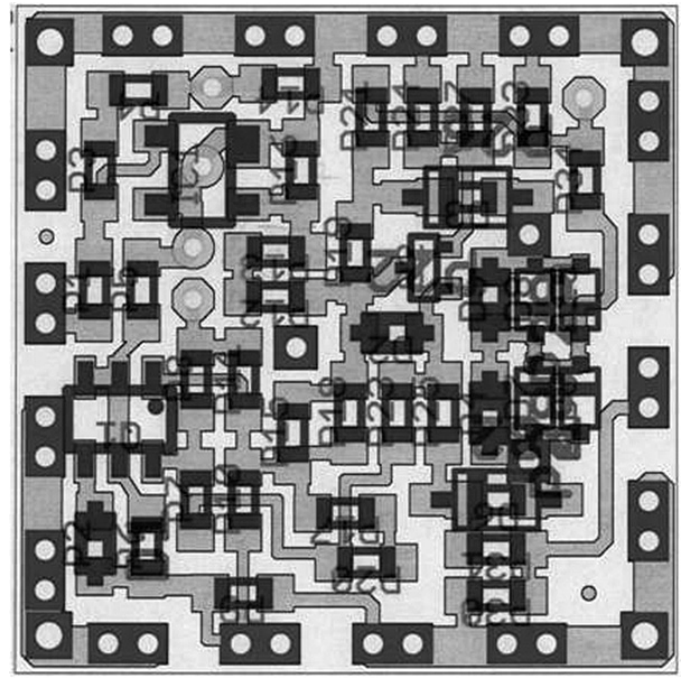

**Figure 8 — Layout of 144 MHz oscillator circuit using LC lumped inductor capacitor resonator network**

## Second Example: 433MHz oscillator circuit

We use the same transistor (BFR193) with, $V_{ce}$ = 8.8V, $I_c$ = 10 mA, $I_B$ = 85 µA, $V_{be}$ = 0.67 V, and we now obtain:

$C_1 = 3.3$ pF, $C_2 = 13$ pF,
$C_{3A} = 7.5$ pF, $C_{3B} = 75$ pF,
$L_E = 13$ nH,
$R_E = 320\ \Omega$, $R_{B1} = 29000\ \Omega$,
$R_{B2} = 20000\ \Omega$,
$C_B = 220$ pF, $C_c = 1000$ pF,
$V_{dc} = 12$ V

resulting an output power of 11.9 dBm and a phase noise of -100 dBc/Hz at 10 kHz offset from the carrier. Since the 144 MHz was about 35 dB better in the phase noise (-135 dBc/Hz at 10 kHz offset), we need to ask why. The phase noise and the carrier frequency are related in a quadratic function. This means three times increase in frequency results in 9 dB degradation in phase noise for 432 MHz oscillator circuit in comparison to 144 MHz oscillator as shown in Figure 7. Therefore, phase noise performance for 432 MHz oscillator circuit should be -126 dBc/Hz instead of -100 dBc/Hz at 10 kHz offset (CAD simulated). The answer is that even in grounded base condition, large signal Re[$Y_{22}$] loads the parallel tuned circuit significantly resulting in a lower dynamic operating Q. We must find a work around for this.

The phase noise and the Q are related in a quadratic function. This means two times the Q results in 12 dB improvements. Since we lost 26 dB, we need to improve the dynamic loaded operating Q approximately 20 times. As this is not possible, there may be more

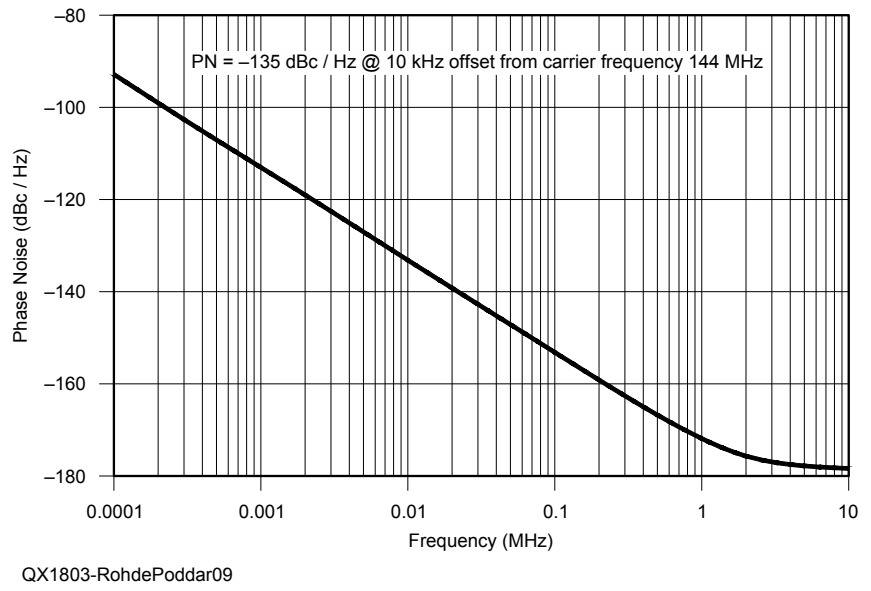


**Figure 9 — Phase noise plot of 144 MHz oscillator reference circuit for the evaluation of the time domain approach.**

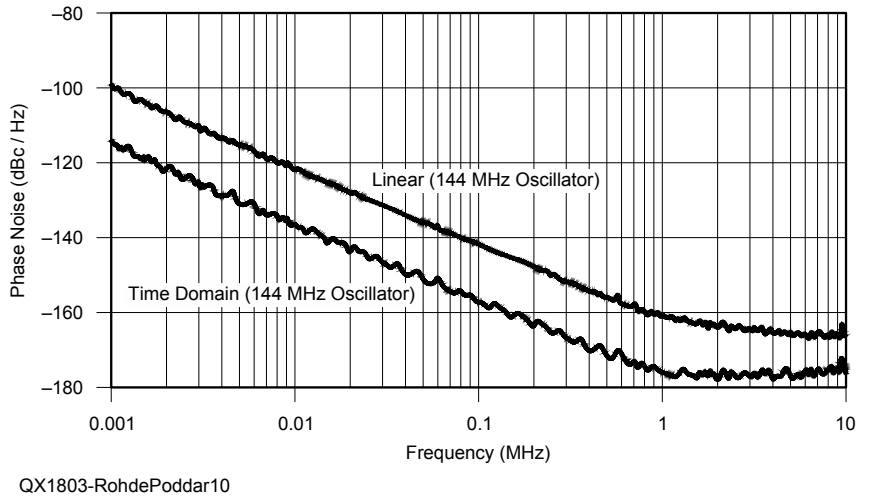


**Figure 10 — The measured phase noise plot for 144 MHz oscillator (linear and time domain).**

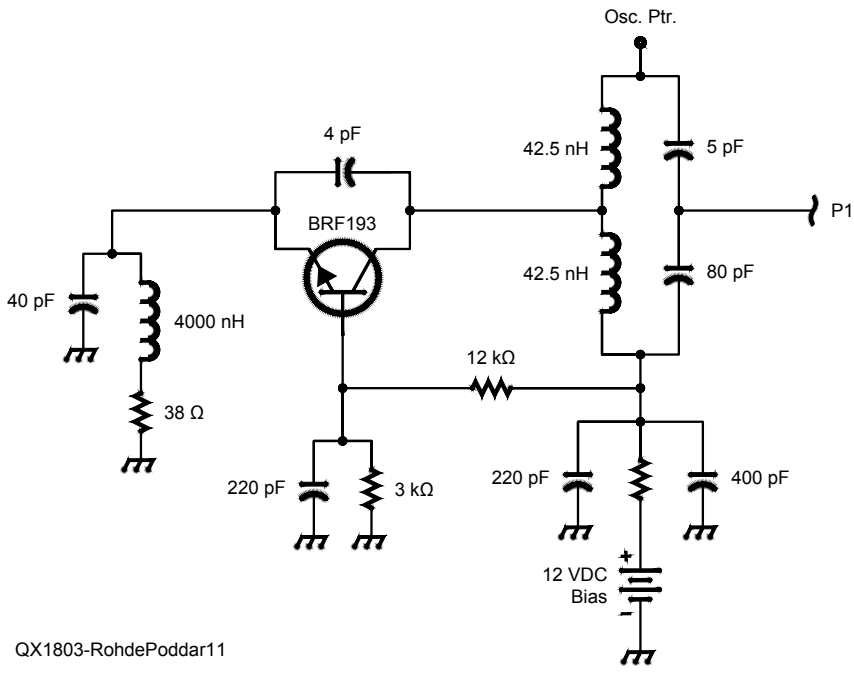


**Figure 11 — Schematic of 432 MHz grounded base oscillator using tapped inductor (30 mA).**

effects than just the Q deterioration. The answer is, "the collector emitter capacitance dynamically detunes the circuit periodically". A solution for this problem is tapping the inductor, therefore decreasing the influence of the transistor. We will show this now.

## Modified Circuit for UHF (432 MHz) and Higher Current

If we inspect $Y_{22}$ of our transistor at 432 MHz and at 30 mA, we will see that the loading of the tank circuit decreases the operating Q significantly. The way around this to apply a center tapped inductor. As the coupling at these frequencies from winding to winding is not extremely high, actually two separate identical inductors can be used successfully.

Figure 11 shows the schematic of a 432 MHz grounded base oscillator using the tapped inductor. This is a modification of the circuit we have used previously. In the case of a VCO, it would be advantageous to use a different output coupling scheme because in this configuration, the loading would vary with frequency. This can easily be achieved by adding some inductive coupling to the circuit. In case of a printed resonator this can be accomplished quite simply.

Figure 12 shows the layout of the 433 MHz oscillator circuit using buried printed coupled line resonator network (stripline resonator: middle layer). The actual resonator would not be visible if the oscillator is visually inspected.

Figure 13 shows the simulated phase noise plot. It shows the expected noise degradation of 9 dB, as the frequency is approximately three times higher. The resulting simulated output power at 432 MHz is 16 dBm, compared to 18 dBm at 144 MHz. This is due to internal package parasitics, which could not be compensated externally. The second harmonic is suppressed by 38 dB; this is due to the higher operating Q.

## Circuit Design Guidelines

The results we have obtained so far were based on mathematical calculations. Some of these calculations are difficult to obtain. However, by inspecting the resulting circuits, there are certain relationship between the values of the capacitance of the tuned circuit and the two feedback capacitors, the collector emitter capacitor and the emitter to ground capacitor. The following shows the set of recommended steps for easy design of such oscillator. Figure 14 shows the typical grounded base oscillator for demonstrating the simple design rules where $C_E$ and $C_F$ are the feedback capacitors that

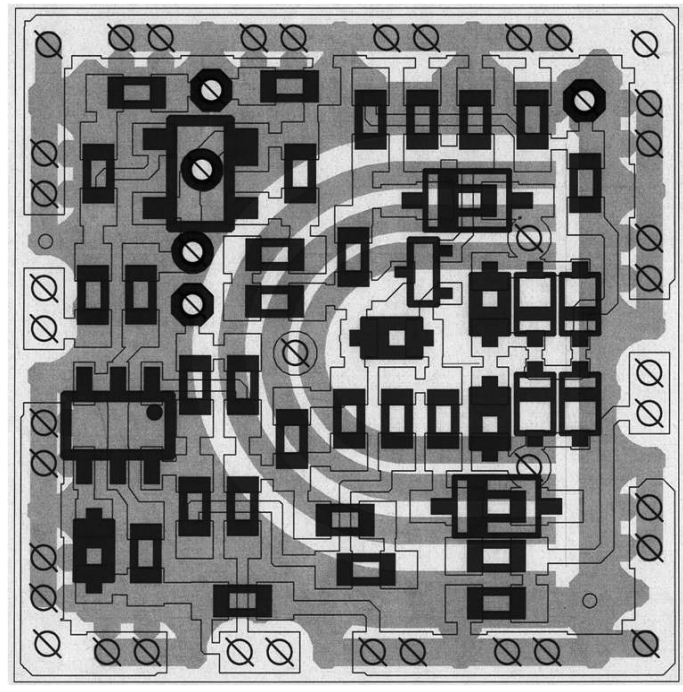

**Figure 12 — Layout of the 432 MHz oscillator circuit using buried printed couple line resonator network (stripline resonator in the middle layer).**

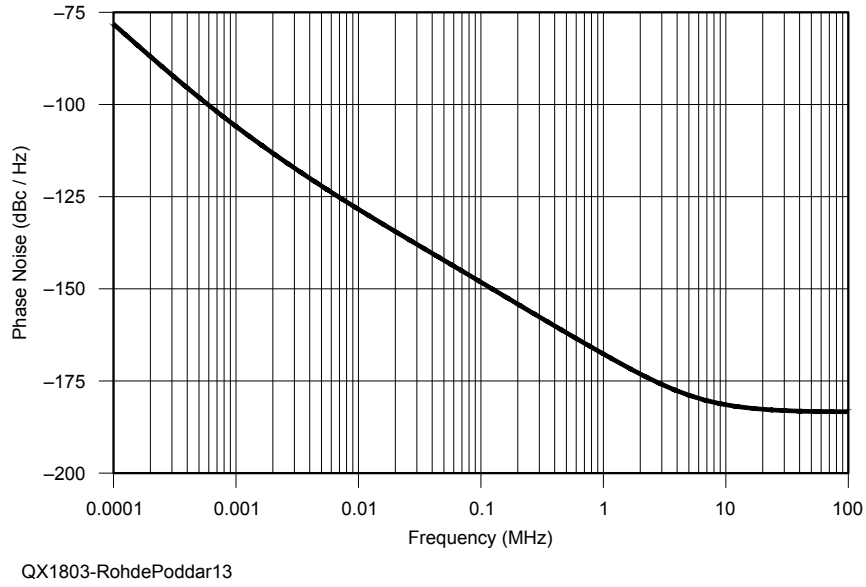


**Figure 13 — The simulated phase noise plot of 432 MHz grounded base oscillator using tapped inductors.**

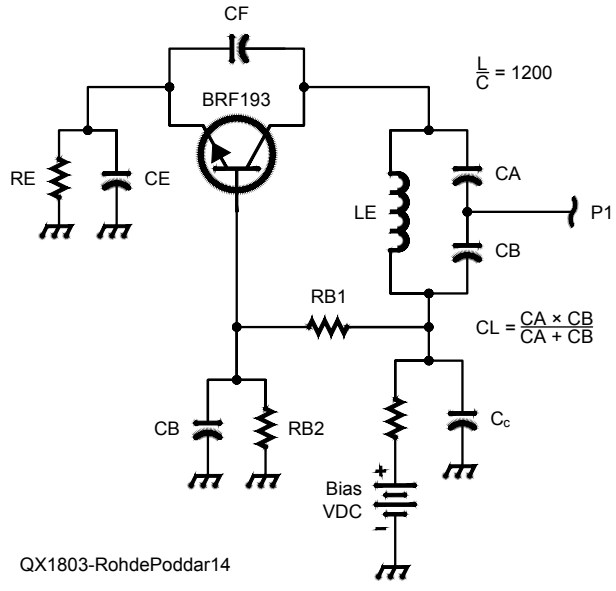


**Figure 14 — Typical configuration of grounded base oscillator circuit.**

generates the negative resistance to compensates the loss resistance of the resonator network comprised of $L_E$ and $C_L^*$.

## Simple Design Rules With an Example:

By setting the *L/C* ratio to a fixed value of 1200 (this is done for optimum energy storage, group delay and energy transfer for a given cycle in the resonator network), the following should be used.

$$\frac{L}{C} = \left[\frac{L_E}{C_L^*}\right]_{Grounded-Base} = 1200$$

$$\Rightarrow Z_0 = \sqrt{1200} \cong 34.6\ \Omega$$

$$L = 1200 \times C$$

$$\Rightarrow L_E = 1200 \times C_L^*$$

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{1200}}$$

$$C_L^* = C_L + \frac{C_E C_F}{C_E + C_F}$$

where $C_E$ ($C_1$) and $C_F$ ($C_2$) are feedback capacitors.

$$C_L = \frac{C_A C_B}{C_A + C_B};$$

where $C_A$ ($C_1$) and $C_F$ ($C_2$) are feedback capacitors.

$C_B = 10\,C_A$.

To examine the accuracy of this simple approach, let us take the same 144 MHz grounded base oscillator as shown in Figure 7.

## Example: The 144 MHz Grounded Base Oscillator

$$C_L^* = \frac{1}{2\pi f\sqrt{1200}} \Rightarrow C \cong 31\ \text{pF}$$

$$L_L = \frac{1}{(2\pi f)^2 C} \Rightarrow L \cong 39\ \text{nH}$$

$C_F = 0.3 \times C_L^* \cong 11$ pF

$C_L = 2 \times C_F \cong 22$ pF

$C_E = 4 \times C_F \cong 44$ pF

$C_A = 22$ pF

$C_B = 220$ pF

These results are comparable with the results above and the calculation is frequency scalable with minor corrections possibly, if necessary. Other alternative short formulas based on linear approximations and published in the literature may not deliver the same high performance.

## Summary

Today's applications, both commercial and consumer, require low cost high performance oscillators and the design time is also very critical. The approach shown here meets these requirements and gives detailed guidelines for better performing oscillators. The concept is explained in detail and validated. This is only one of the many applications for which this technique is applicable. Furthermore, by translating this design to integrated circuits very high performance but very low cost oscillators can be made. From a theoretical point, we found it surprising that simple equations could be found which optimized the design and accurately predicted the phase noise. For the determination of the output power, a nonlinear CAD tool is recommended if the frequencies are higher than 500 MHz. Our example has shown that at frequencies below 200 MHz the output power can be determined quite accurately using this approach.

To make this oscillator part of a PLL synthesizer, electronic tuning is required. The output capacitor should then have a set of tuning diodes in parallel , with light coupling , to properly select the tuning range.



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