# Monolithic Microwave Integrated Circuits

***Part 2:*** Last month, we learned about MMICs and simple applications. This month, we will see how to combine these devices for more power output and look at important performance characteristics.

By Al Ward, WB5LUA
Rte 9, Box 132
McKinney, TX 75069

Last month, I showed how easy it is to cascade MMICs for increased gain. The next logical question is "How can I increase the power-output capability of these devices?" Since the 01 through the 04 series MMICs are unconditionally stable, it is easy to parallel two or more devices for increased power output. The 1-dB compression point for two devices in parallel is almost 3 dB greater than that for a single device. For four devices in parallel, the 1-dB compression point is about 6 dB greater! Of course, the gain of a paralleled-MMIC amplifier will be no greater than that of a single device; in fact, the gain may be slightly lower because of losses in the divider/combiner networks.

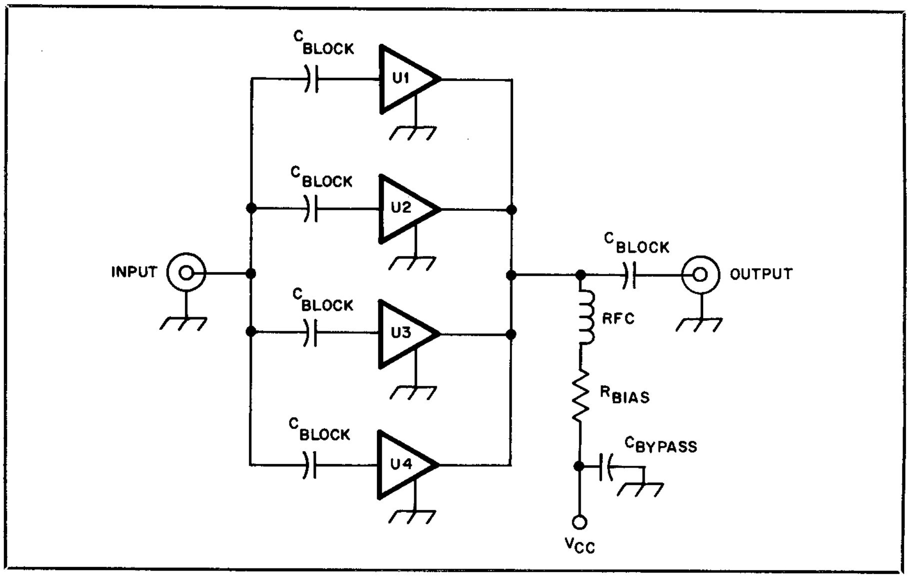



Fig 1—The simplest form of parallel-MMIC amplifier ties the inputs and outputs of the devices together. Input and output impedances are 50/4 = 12.5 ohms, so some sort of impedance matching is desirable if this amplifier is to be used in a 50-ohm system.

### A Simple Amplifier

In its simplest form, a four-MMIC amplifier can be built as shown in Fig 1. Amplifier input and output impedances will be approximately 50/4 = 12.5 ohms. The input of each MMIC must have a dc blocking capacitor for isolation from the other MMICs, but the outputs can be connected together directly. Dc is applied through a common RF choke and a series bias resistor of appropriate resistance and power rating. A single blocking capacitor is used on the output.

Since it is normally desirable to retain a nominal 50-ohm input and output impedance, some sort of matching circuit is required. For maximum bandwidth at HF, simple toroidal transformers may be used. This concept is shown in Fig 2. The transformers supply equal-amplitude signals that are 180 degrees out of phase. These 1:1 transformers are typically called baluns and lend themselves to push-pull operation rather easily. Amplifier bandwidth will be determined mainly by the frequency response of the transformer, not the MMIC. The RF choke in the output network is included to allow all four MMICs

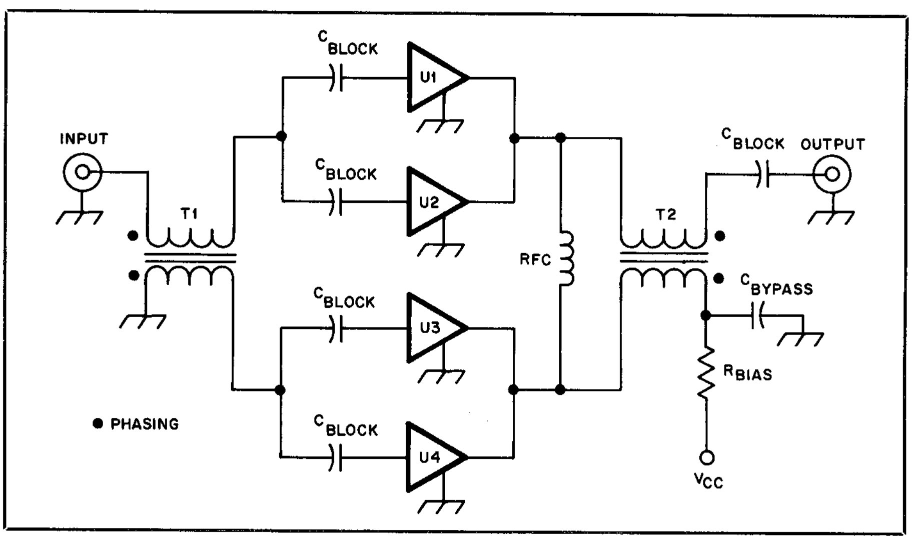



Fig 2—For use at HF, the basic four-MMIC amplifier can be paralleled in a push-pull configuration and matched to 50 ohms with 1:1 transformers. $C_{BLOCK}$ and $C_{BYPASS}$ should have a low reactance at the frequency of operation, while the RFC should have a high reactance. The bias-resistor value will depend on which MMICs are used.

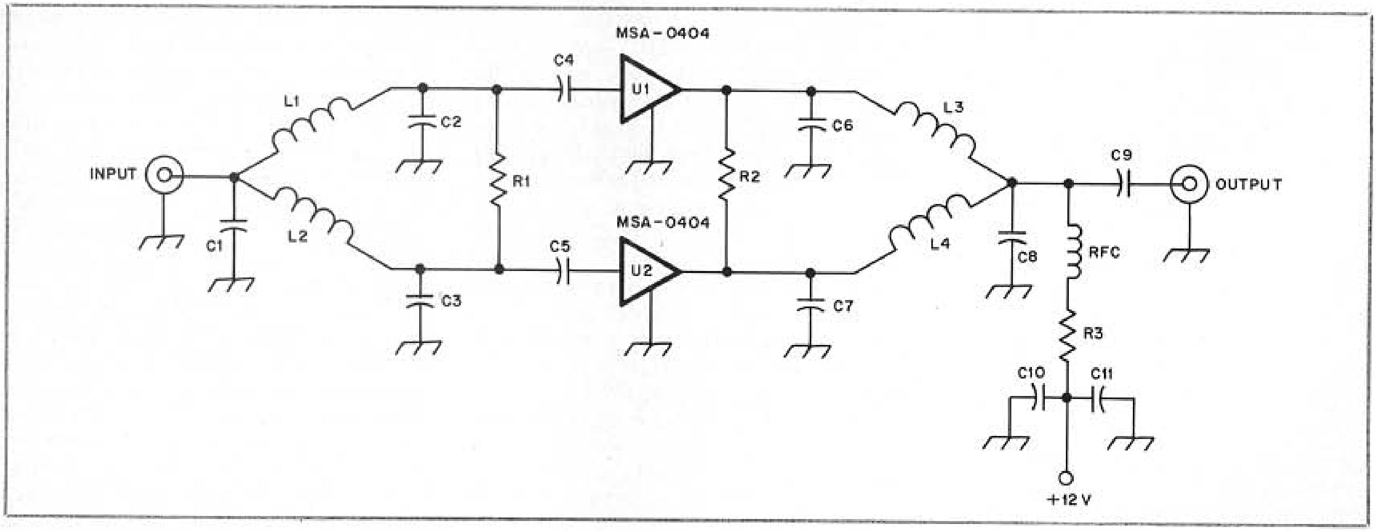



Fig 3—For VHF, MMICs in parallel may be matched to 50 ohms with Wilkinson divider/combiner networks. This amplifier may be built for 220 or 432 MHz. See text and Table 1.

to be fed from a single bias resistor.

**Parallel MMICs at VHF**

At VHF, impedance matching for a parallel-MMIC amplifier can be accomplished with Wilkinson-type power divider networks. A circuit that uses lumped elements to combine two MMICs is shown in Fig 3. Eqs 1-4 can be used to calculate element values for single-section Wilkinson power dividers in a 50-ohm system at any frequency of interest. The values for L1-L4 are:

$$L = \frac{70.7}{2\pi F_o} \qquad \text{(Eq 1)}$$

where

$L$ = inductance in henrys

$F_o$ = frequency of operation in hertz

For C2, C3, C6 and C7:

$$C = \frac{1}{2\pi F_o 70.7} \qquad \text{(Eq 2)}$$

where

$C$ = capacitance in farads

$F_o$ = frequency of operation in hertz

For C1 and C8:

$$C = 2\,C2 \qquad \text{(Eq 3)}$$

For R1 and R2:

$$R = 2\,Z_0 \qquad \text{(Eq 4)}$$

where $Z_0$ = the nominal impedance in ohms. $Z_0$ will always be 50 ohms in MMIC circuits, so R1 and R2 will always be 100 ohms. An in-depth description of Wilkinson power dividers appeared in *Ham Radio* several years ago.[1]

C4, C5, C9 and C10 should have a low reactance (less than several ohms) at the frequency of operation. The RF choke should have a reactance such that when added to the series-bias-resistor value, the total value will be approximately 10 times the output impedance, or 500 ohms. C11 is a low-frequency bypass capacitor.

At amateur frequencies up to 225 MHz, the lumped-constant Wilkinson power divider approach works well with MMICs. Above 225 MHz, the performance may not be as expected for several reasons. First, the capacitor values as calculated are small (less than 10 pF); with standard components it may be hard to achieve the exact value. Second, dipped silver-mica capacitors that exhibit their marked value at low frequencies (1 MHz) may not necessarily exhibit the same value at 400 MHz because of parasitic components such as lead inductance or shunt reactance.

A third, and not so obvious, reason is that although MMICs typically have a nominal 50-ohm input and output impedance, it may not be exactly 50 ohms resistive. When an MMIC is designed to operate over a very wide bandwidth, the circuit values inside the MMIC package are chosen so that the gain, as measured in a 50-ohm system, is relatively constant over a wide frequency range. As a result, the input and output match may not be optimum at any frequency. If the input and output impedance at each frequency is plotted on a Smith Chart, the plot resembles a circle whose center would be near 50 ohms resistive. Since the devices are somewhat reactive, they have the effect of changing the resonant frequency of the Wilkinson networks. The Wilkinson network is generally lowpass by design, so it follows that if the network were designed for a slightly higher frequency, the MMIC amplifier may not require any further tuning.

**Test Amplifiers for 220 and 432 MHz**

To analyze the basic concept of the Wilkinson divider, I designed and tested a 220-MHz version of the amplifier shown in Fig 3 using the values shown in Table 1. Dipped silver-mica capacitors of the closest standard value to the calculated value were used for the matching elements. L1 through L4 are each four turns of no. 24 wire, 0.125-inch ID, spaced one wire diameter. Leads 0.25 inch are included in the design to facilitate mounting. See Fig 4.

A swept-frequency-response plot showing gain and reverse isolation for the

**Table 1**

**Component Values for the Circuit of Fig 3**

| | *220 MHz* | *432 MHz* |
|---|---|---|
| C1, C8 | 20-pF SM | 1-10 pF (variable) |
| C2, C3, C6, C7 | 10-pF SM | 5-pF SM |
| C4, C5, C9, C10 | 470-pF SM | 100-pF SM |
| C11 | 0.1 μF | 0.1 μF |
| L1-L4 | 50 nH (see text) | 26 nH (see text) |
| R1, R2 | 100 Ω | 100 Ω |
| R3 | 62 Ω, 1 W | 62 Ω, 1 W |
| RFC | 0.47 μH | 0.47 μH |
| U1, U2 | MSA-0404 | MSA-0404 |

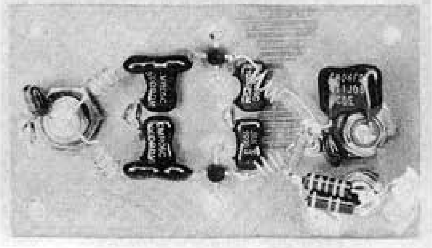


Fig 4—A 220-MHz version of the amplifier shown in Fig 3 can be built on unetched PC-board material.

[1]E. Franke, "Wilkinson Hybrids," *Ham Radio*, Jan 1982, pp 12-18.

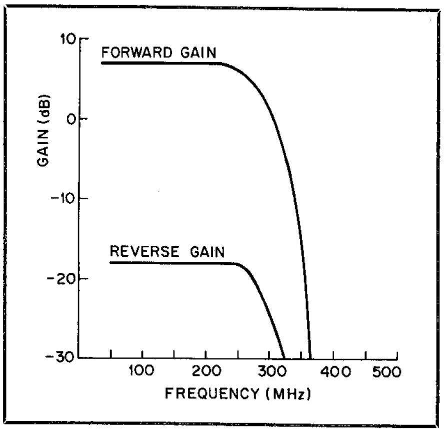



Fig 5—Gain of the 220-MHz MMIC amplifier shown in Fig 4 is almost flat below the design frequency but falls off rapidly above it. This graph shows both forward and reverse gain.

220-MHz amplifier is shown in Fig 5. Reverse isolation (S12) is indicative of amplifier stability. In the case of the 220-MHz amplifier, stability is quite good since −S12 is 11 dB greater than S21. If −S12 were no greater than S21, stability would be marginal. As mentioned earlier, the response is lowpass in nature. Gain is similar to that of a single device, while the 1-dB compression point is +16 dBm (40 mW) and the compressed output will be more than +18 dBm (63 mW).

If greater gain is desired at the expense of power output capability, the 01, 02 or 03 series devices can be paralleled instead of the 04 devices. This concept will work fine down to HF as long as appropriate element values are calculated and appropriate blocking and bypass capacitors and RF choke are chosen.

A similar amplifier was designed and built for 432 MHz using the element values determined from the preceding equations. Component values are shown in Table 1. L1 through L4 are each 1.5 turns of no. 24 wire, 0.125-inch ID, spaced one wire diameter. Inductor leads are 0.25 inch long. During construction and testing, I found that if C1 and C8 were made variable, gain could be peaked at 432 MHz and input and output SWR could be minimized.

The response of the amplifier built and tuned as described here is shown in Fig 6. Gain is flat down to 200 MHz (gain was not measured below 200 MHz), and input and output SWR are also quite acceptable. Allowing C1 and C8 to be variable allows you to tune out the reactive component of the MMIC and in fact does produce additional gain over the untuned 220-MHz amplifier just described. The 432-MHz amplifier is capable of power output similar to the 220-MHz amplifier.

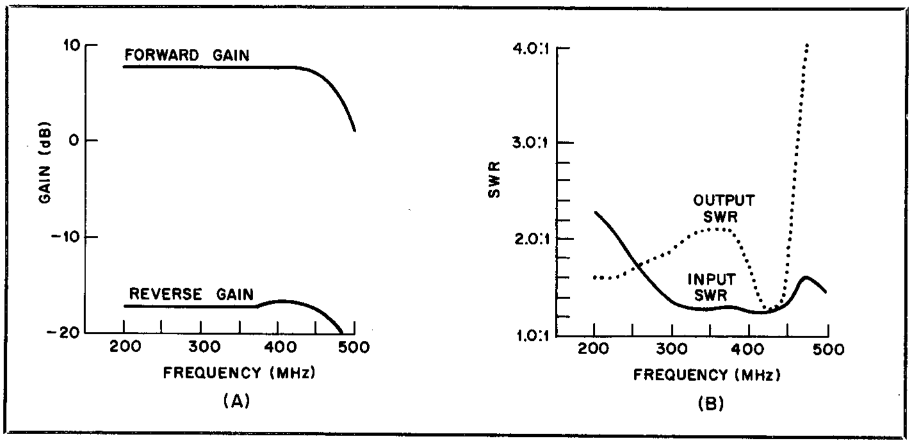



Fig 6—Gain response (A) of a 432-MHz version of the amplifier of Fig 3 is good down to at least 200 MHz. Part B shows that the input and output SWR is best at the design frequency.

**Techniques for 902 MHz and Above**

Although the paralleled MMICs work very well at HF and VHF, the real advantages don't show up until they are applied at 902 MHz and higher. At microwave frequencies, the transmission line equivalent of the Wilkinson power divider is constructed very easily. Two possible options are shown in Fig 7.

The transmission line is a quarter wavelength long at the frequency of operation, and its characteristic impedance is determined from

$$Z_0 = \sqrt{Z_{in} \times Z_{out}} \quad \text{(Eq 5)}$$

where $Z_{in}$ and $Z_{out}$ are the impedances to be matched.

For the two-MMIC amplifier shown in Fig 7A, the 50-ohm nominal impedance of the MMIC has to be transformed to

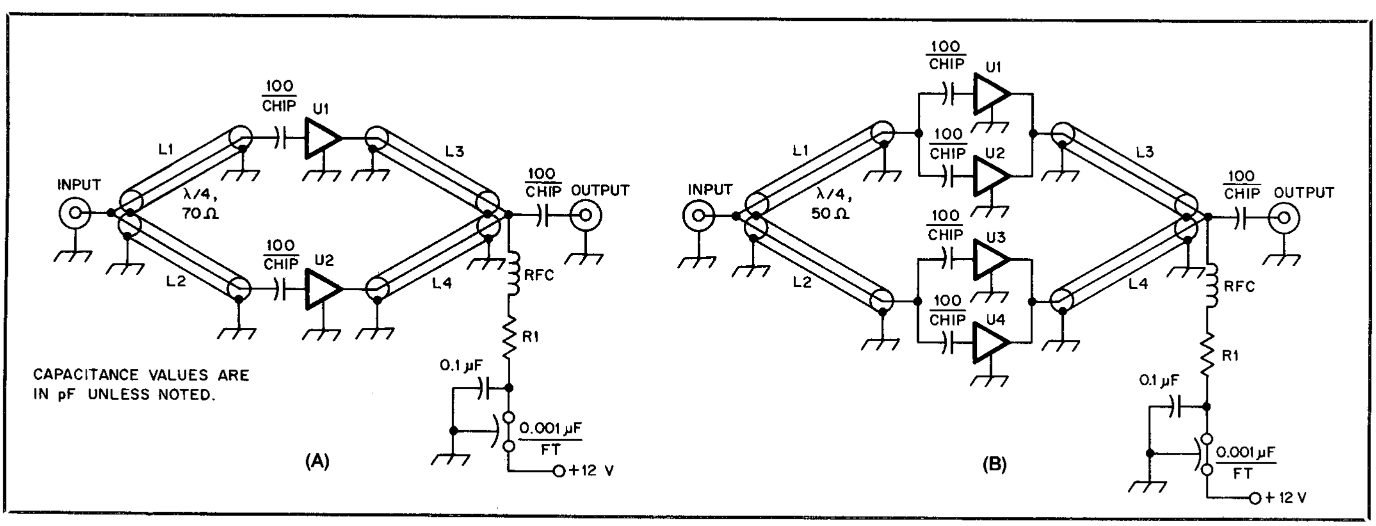



Fig 7—At 902 MHz and above, ¼-wavelength transmission lines replace the lumped elements in the Wilkinson dividers. The circuit at A, for two MMICs, uses 70-ohm lines, while the four-MMIC amplifier at B uses 50-ohm lines. Line lengths for various frequencies are shown in Table 2. All 100-pF capacitors are 50-mil or 100-mil RF-type ceramic chips.

L1-L4—See text and Table 2.
R1—For the circuit in A: 62 Ω, 1 W. Set for 100-mA idling current. For the circuit in B: 40 Ω, 2 W. Set for 200 mA idling current.
RFC—6t no. 24 wire, 0.125-in ID, spaced 1 wire diam.
U1-U4—Identical MMICs. MSA-0404 recommended for maximum power output.

100 ohms so that two of these networks can be paralleled to yield 50 ohms. Therefore, the characteristic impedance of the transmission lines should be

$$Z_0 = \sqrt{50 \times 100} = \sqrt{5000}$$
$$= 70.7 \text{ ohms}$$

For the four-MMIC circuit of Fig 7B, two MMICs are first paralleled to yield 25 ohms and then transformed to 100 ohms. This is done so that two of these networks can be paralleled to obtain a nominal 50-ohm impedance. Therefore, the characteristic impedance of the transmission lines for this circuit is

$$Z_0 = \sqrt{25 \times 100} = \sqrt{2500} = 50 \text{ ohms}$$

Identical transmission-line networks are used for both input and output matching. No tuning is required. The 50-ohm and 70.7-ohm transmission lines can be constructed from coaxial cable or simulated in a microstripline configuration. Table 2 shows the length of the ¼-wavelength lines for several frequencies. Above 2 GHz, correction had to be made to the cable length to compensate for end effects and parasitics. The cable dimensions are measured shield end to shield end.

**Table 2**

**Lengths of ¼-Wavelength Lines For UT-141 Cable**

| *Frequency (MHz)* | *Length (Inches)* |
|---|---|
| 902 | 2.3 |
| 1296 | 1.6 |
| 2050 | 0.9 |
| 2304 | 0.8 |

The circuit of Fig 7B is very attractive since low-loss, 50-ohm 0.141-inch semirigid cable is readily available and allows four MMICs to be paralleled easily. The 1-dB gain-compression point will be 5 to 6 dB greater than with a single MMIC. I recommend using the MSA-0404 MMIC in the parallel amplifiers because it offers the highest power output of any of the inexpensive plastic devices. Measured power output at the 1-dB gain-compression point for an assembly of four MSA-0404s is +19 dBm at 1296 MHz and +17 dBm at 2304 MHz. At 902 MHz, +19 dBm should be achieved easily. Saturated power output has been measured at more than +20 dBm (100 mW) at 1296 MHz and +18 dBm (60 mW) at 2304 MHz.

Gain at 1-dB gain compression measures 5 dB at 1296 MHz and 4 dB at 2304 MHz. These amplifiers have gain over a broad frequency range. The usable bandwidth of the 1296-MHz model is 300 MHz.

**Construction of a 1296-MHz Amplifier**

Fig 8 shows the layout of a 1296-MHz version of the four-MMIC amplifier of Fig 7B. It is built on a 2.05- × 4.05-inch piece of 0.062-inch-thick, glass-epoxy, double-sided circuit board. The board is not etched on either side and acts as a convenient circuit ground plane. This board will fit nicely into the lid of an aluminum diecast box (Bud CU-124 or Hammond 1590B). SMA connectors are desirable because of their small size and good UHF characteristics. Use screws or small wires to attach the flange (ground connection) of the SMA connector to the ground plane on the component side of the board. The ground must be carried through the board to ensure good RF performance.

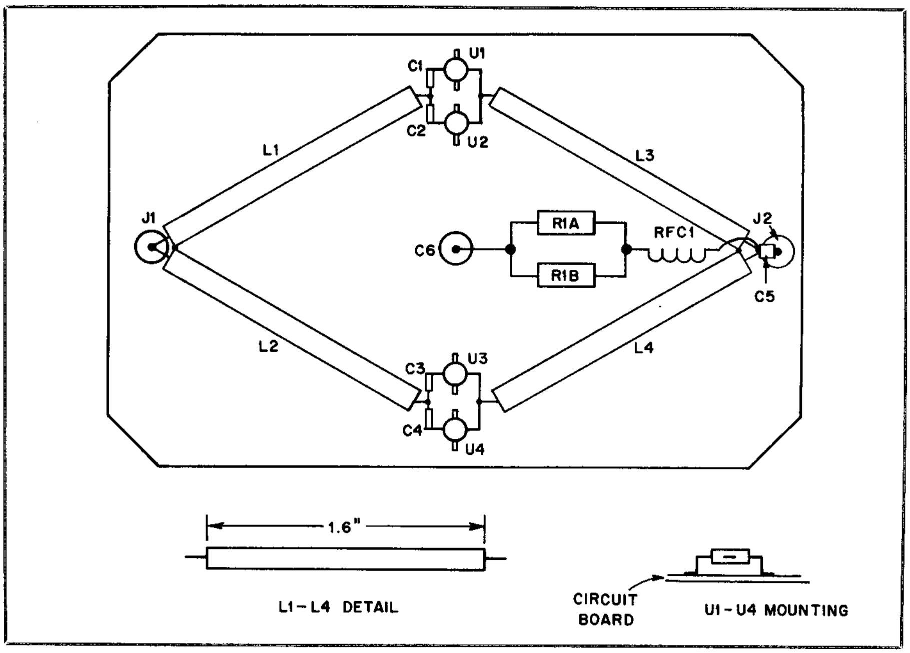



Fig 8—Board layout for a 1296-MHz version of the amplifier shown in Fig 7B.

The transmission lines are made from miniature 50-ohm, 0.141-inch, semirigid coaxial cable (UT-141). Cut each piece so that the outer jacket is 1.6 inches end to end. All four cables should be cut to the same length within ±0.020 inch, which amounts to slightly over ±1 electrical degree at 1296 MHz. Excessive differences in cable length contribute to a phase error which will prohibit the outputs of the four MMICs from adding in phase and producing maximum power output. Tack solder the ends of each piece of UT-141 cable to the ground plane. Soldering along the entire length of the cable jacket is not required.

Be very careful when handling MMICs; the leads may break off if they are bent directly at the case. Use the lead from a 1-W resistor as a tool to form the leads of each device as shown in Fig 8. Use a 15-W soldering iron to tack solder the ground leads to the ground plane and to solder the input and output leads. Mount the devices so that the center-to-center distance is 5/16-inch maximum. This way, the 0.1-inch-square chip capacitors can be mounted between the UT-141 center conductor and the device input. A very short length of no. 24 wire can be used to tie the MMIC outputs and the UT-141 center conductor together. When laying out the board, be sure to leave enough room for C5 near the output connector.

**A 2304-MHz Microstripline Amplifier**

At 2304 MHz, inexpensive MMICs can be used to reach a power level of 50 mW or so, enough for local QSOs and even DX contacts under the right conditions. There are, however, some design considerations to be aware of. As we begin to cascade the MMIC amplifiers, we need to make sure that it is the final output stage that begins to compress first. If a driver stage were to compress first, it might be difficult, if not impossible, to drive the final to the desired power output. In addition, intermodulation distortion (IMD) products will increase. As a rule of thumb with identical devices, if one MMIC is used to drive two MMICs, the gain of each MMIC should be greater than 3 dB and preferably 6 dB. If the gain of each device were 3 dB in a one-driving-two circuit, the driver and output stages would reach the 1-dB gain-compression point at the same time. The result would be an amplifier with a 2-dB gain-compression point where 1-dB gain compression was desired. In a one-driving-four MMIC circuit, the gain of each MMIC should be greater than 6 dB, and preferably 9 dB.

Herein lies the design problem associated with the inexpensive MSA-0404. The gain at 2304 MHz is only 5-6 dB. One 0404 driving four 0404s would result in a 1-dB gain-compression point of only +15 to +16 dBm, a compromise because +17 dBm is possible. The problem is solved by using one MSA-0404 to drive a pair of MSA-0404s and then using each one

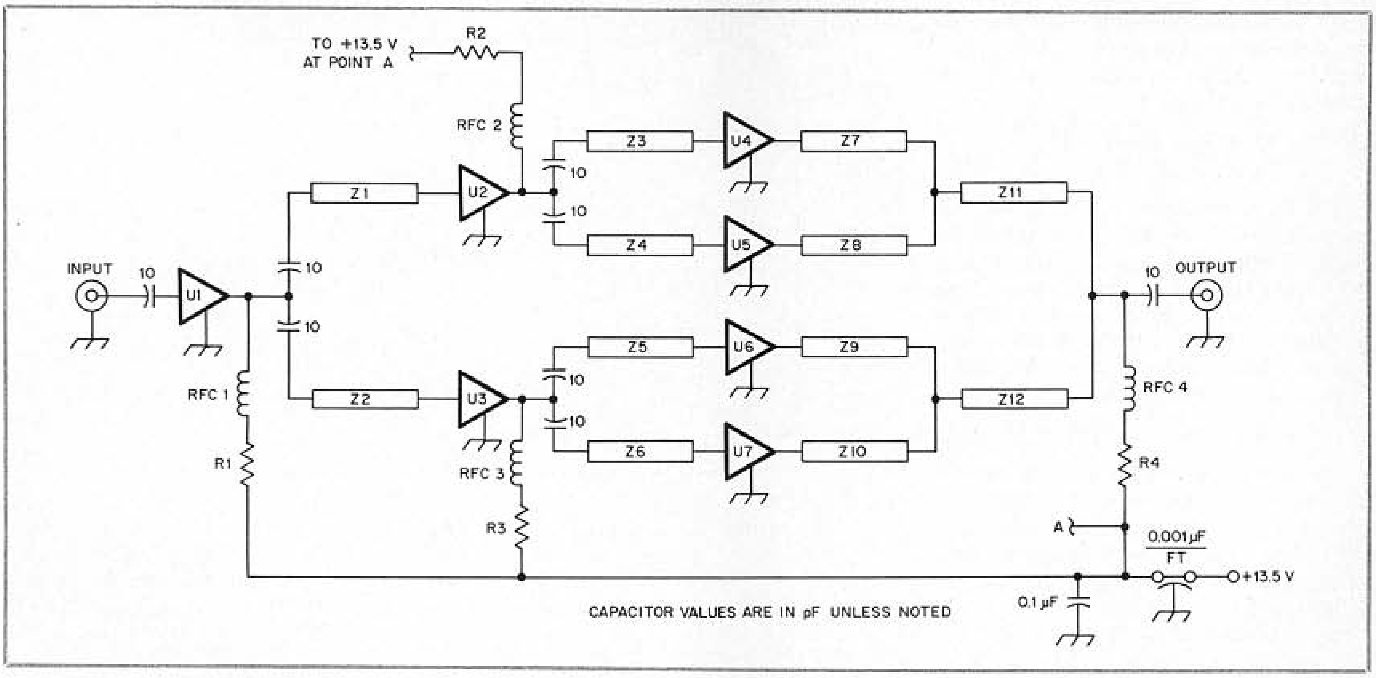



Fig 9—Schematic of a 2.3-GHz microstripline amplifier using seven MSA-0404 MMICs. All 10-pF capacitors are 50-mil or 100-mil RF-type ceramic chips.

R1-R3—150-Ω, ½-W carbon resistor.
R4—30-Ω, 2-W (minimum). Made from five 150-Ω, ½-W carbon resistors in parallel.
RFC1-RFC4—6t no. 28 wire, 0.125-in ID, spaced 1 wire diam.
U1-U7—MSA-0404 or MSA-0485 MMICs.
Z1-Z12—Etched ¼-wavelength, 70-ohm microstriplines. See text and Figs 10 and 11.

of the pair to drive another pair of MSA-0404s. The outputs are then recombined to give a single 50-ohm output. The divider and combiner networks can be constructed of 70-ohm microstriplines in a Wilkinson power divider configuration. This concept is shown schematically in Fig 9 and photographically in Fig 10.

The microstripline network is realized by using double-sided, 0.031-inch-thick Duroid® 5880 or 3M material with a dielectric constant of 2.17. The 50-ohm transmission lines are 0.120-inch wide, while the 70-ohm transmission lines are 0.060-inch wide. An etching pattern and parts-placement diagram are shown in Fig 11. Copper is retained on the bottom side for use as a ground plane. The etched board fits nicely in the lid of a Bud CU-124B diecast aluminum box. Space restrictions dictated the use of six-turn RF chokes rather than etched quarter-wavelength bias-decoupling lines. As it turns out, this may have contributed to the excellent bandwidth obtained with this design.

The performance of the unit was as expected at 2304 MHz. Gain was measured at 17 dB, and the power output at 1-dB gain compression was measured at +17 dBm (50 mW). Saturated power output was 60 mW. I wanted to get some idea of bandwidth of this unit, so I had the gain measured on a Hewlett-Packard HP 8409 automatic network analyzer. To my amazement, the gain went up to 19 dB at 2 GHz and 21 dB at 1296 MHz. I could achieve a saturated power output of

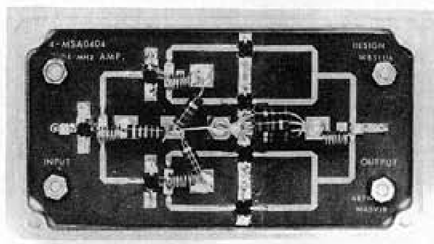
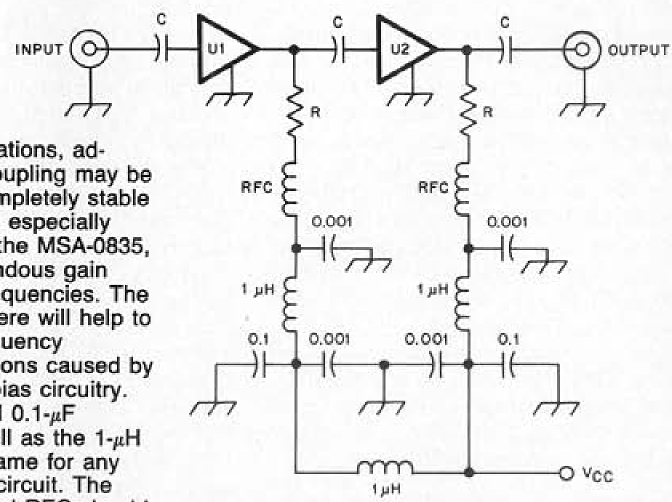


Fig 10—The finished 2.3-GHz, seven-MMIC amplifier fits neatly in the lid of a standard diecast box.

100 mW at 1296 MHz. Even though the matching networks were designed to be resonant at 2304 MHz, the rejection below 2304 MHz is offset by an increase in MMIC amplifier gain and a reduction in MMIC input and output SWR. The result is a 3-dB gain bandwidth of more than 2 GHz as shown in Fig 12. Input SWR is less than 1.6:1 between 500 MHz and 3 GHz, while the output SWR is 1.9:1 at 2304 MHz and increases with decreasing frequency.

The wide bandwidth of this amplifier




In some applications, additional bias decoupling may be necessary for completely stable operation. This is especially true when using the MSA-0835, which has tremendous gain (30 dB) at low frequencies. The network shown here will help to minimize low-frequency (HF/VHF) oscillations caused by feedback in the bias circuitry. The 0.001-µF and 0.1-µF capacitors, as well as the 1-µH chokes are the same for any cascaded MMIC circuit. The values of C, R and RFC should be chosen for proper MMIC operation at the desired frequency, as explained elsewhere in this article.

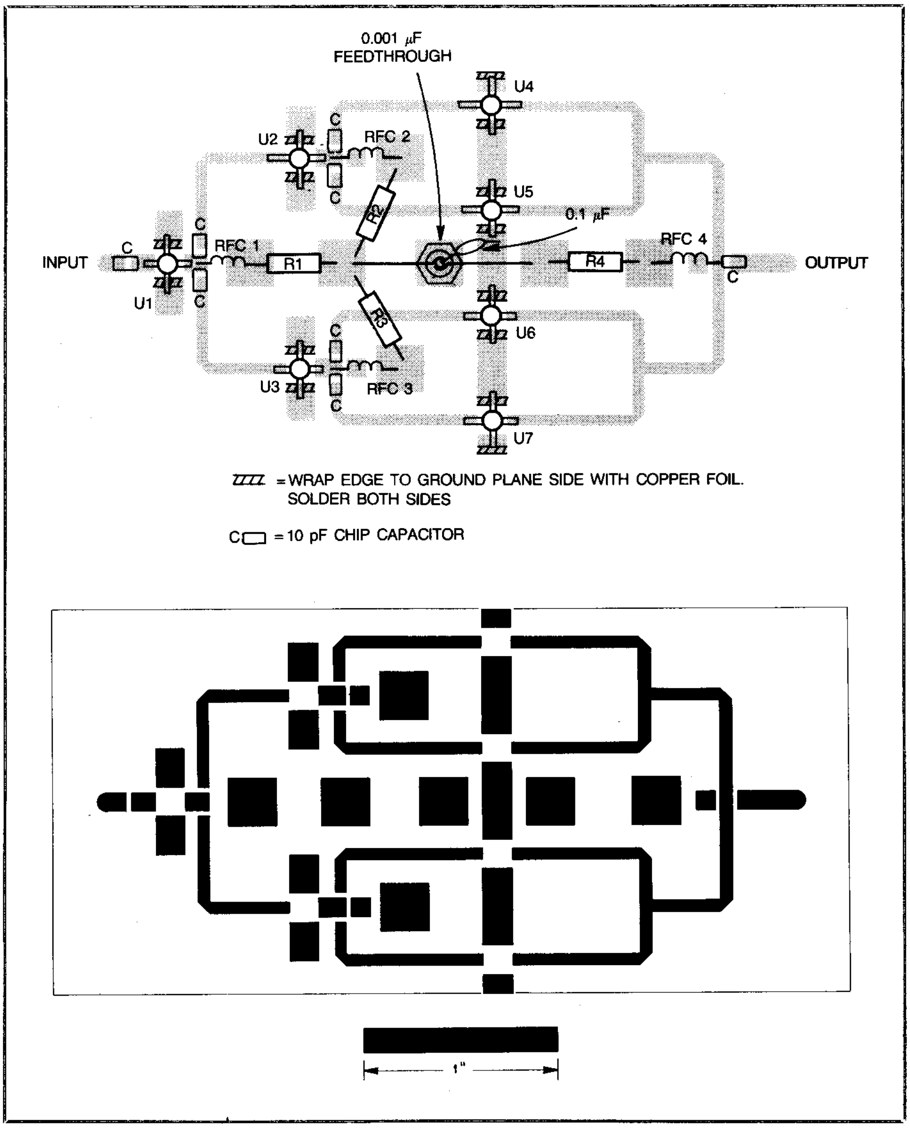



Fig 11—Etching pattern and parts-placement guide for the 2.3-GHz amplifier of Fig 9. The board layout is for 0.031-inch-thick, double-sided Duroid 5880 material ($E_r$ = 2.17). The artwork must be revised if PC-board material with a different dielectric constant is used. One side of the board is left unetched to act as a ground plane. All components mount on the etched side of the board.

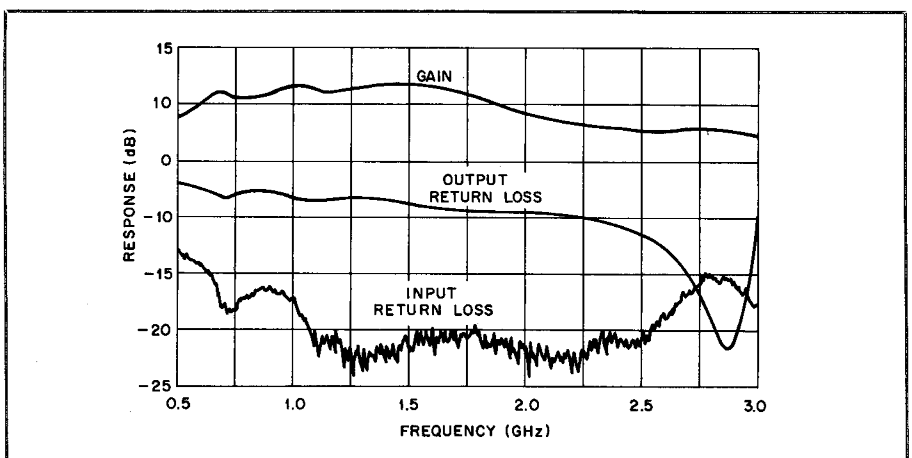



Fig 12—Gain, input return loss and output return loss of the 2.3-GHz MMIC amplifier show that this amplifier is usable from 500 MHz to 2.5 GHz.

makes it usable on several amateur bands. Remember that all this performance comes from an amplifier with no tuning! Total MMIC cost is only $21 for the seven 0404s and less than $14 if the new MSA-0485s are used. Gain for the 0485 version will even be slightly higher. Each MMIC draws 50 to 60 mA, so combined current drain is about 350 mA. Current requirements are the same with or without drive since the amplifier is running class A.

**Construction**

Construction is similar to that of the 1296-MHz amplifier described earlier and the microstripline amplifier described in Part 1 of this article. The etched PC board fits nicely into the lid of a diecast aluminum box. Clear away some ground-plane copper (approximately 0.130 inch) around the hole for each SMA-connector center pin and solder the connector flange to the PC-board ground plane. Drill holes in the box lid to clear the connectors. A feedthrough capacitor supplies $V_{cc}$ to the amplifier.

Connect the MMIC common leads to ground using the techniques described in Part 1 of this article. Chip capacitors should be good 0.05- or 0.10-inch-square RF types, such as those manufactured by Dielectric Labs or ATC.

**Predicting MMIC Amplifier Performance**

It's very easy to cascade and/or parallel MMICs for a wide variety of applications. When deciding which (and how many) devices to use to fill a given need, it is helpful to do a little homework first. Predicting the performance of an amplifier made from a given combination of MMICs is merely a matter of understanding a few basic parameters: gain, SWR, noise figure, 1-dB gain compression, and intercept point.

When dealing with transmitter stages, generally all parameters except noise figure are considered important. Since the noise figure for most MMICs is in the 5-6 dB range, the noise level is so low that other levels in the exciter such as carrier suppression and phase noise are the most dominant factors. In a receiver, all parameters should be considered if good dynamic range is desired. The intent of this section is simply to review these concepts and give several examples. Actual system requirements will be left up to the builder.

**Gain**

Gain is a measurement of the difference in power available at the source and power available after the device under test (DUT) is inserted. This is shown in Fig 13. To get the most accurate gain measurements possible, the source impedance and the power measuring instrument should exhibit a low SWR (less than 1.15:1) referred to the system impedance (50 ohms in this case). Occasionally the impedance of the signal source or power meter is not 50 ohms resistive. A 50-ohm, 6- to 10-dB attenuator can be used between the DUT and test

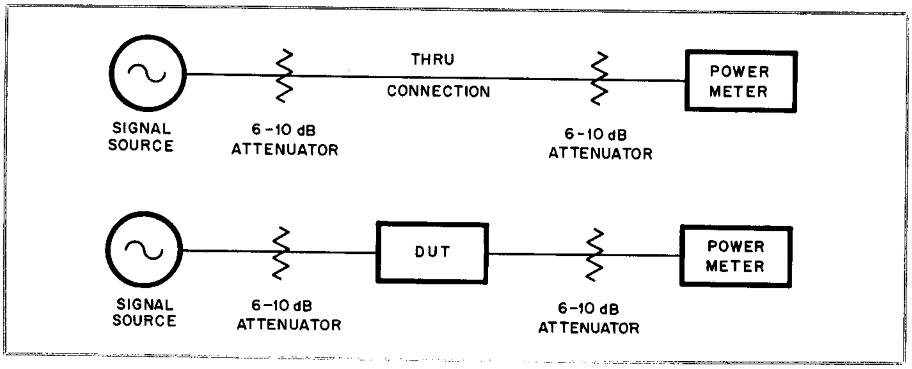



Fig 13— A test setup for measuring gain is first calibrated without the amplifier (DUT) in line. The 6-10 dB attenuators ensure adequate impedance matching of all components to 50 ohms.

equipment to obtain an adequate impedance match.

Since we are making a gain measurement with the "available power" method (which, by the way, is the standard accepted industry method), the effect of the DUT input and output SWR is automatically taken into account with the gain measurement. Included in the gain measurement of the DUT is the mismatch loss which is associated with the SWR of the DUT. Mismatch loss (ML) can be calculated from:

$$ML = -10 \log \left[1 - \left(\frac{SWR - 1}{SWR + 1}\right)^2\right] \quad \text{(Eq 6)}$$

If the input and output SWR is 1.0:1, then the corresponding mismatch loss is 0 dB. Any improvement in the input and output SWR of an amplifier results in an increase in measured gain equal to the reduction in mismatch loss at each port.

When cascading MMICs, we would like to see the resultant measured gain equal to the sum of the individual MMIC gains. This would be possible if the input and output SWR of each MMIC were 1.0:1. However, this is rarely the case. Eq 7 can be used to calculate mismatch loss as a function of two SWRs beating against one another.

Mismatch Loss =

$$20 \log\left[1 \pm \left(\frac{SWR_1 - 1}{SWR_1 + 1} \times \frac{SWR_2 - 1}{SWR_2 + 1}\right)\right] \quad \text{(Eq 7)}$$

The resultant mismatch loss will either add to or subtract from the sum of the individual MMIC gains. The + term in Eq 7 will give the maximum possible additional loss, while the − term will give the minimum possible additional loss (which is in reality gain). Maximum mismatch loss will occur at some electrical spacing, L, between the two MMICs. Minimum loss will occur at a spacing ¼ λ shorter or longer than L. It is possible for two SWRs (>1.0:1) to be a conjugate match (that is, R +*j*X and R −*j*X on the Smith Chart). If this occurs, the cascaded MMICs will produce more gain than the sum of the gains of the individual MMICs would indicate is possible.

For example, two 1.5:1 SWRs could produce 0.34 dB additional loss, or 0.35 dB less loss (more gain) than the sum of the individual amplifier gains. Suppose an amplifier has two cascaded MMICs. The output SWR of MMIC no. 1 is 2.0:1, and the input SWR of MMIC no. 2 is 1.5:1. Assume the input SWR of MMIC no. 1 and output SWR of MMIC no. 2 to be 1.0:1. The mismatch loss could be +0.56 dB maximum or −0.6 dB minimum. If the gain of MMIC no. 1 is 6 dB and the gain of MMIC no. 2 is 7 dB, the possible resultant gain of the cascaded pair could be

6 dB + 7 dB + 0.56 dB = 13.56 dB maximum gain

or

6 dB + 7 dB − 0.6 dB = 12.4 dB minimum gain.

The actual gain will be between 12.4 and 13.56 dB, depending on the electrical length between the two devices. Eq 7 gives an idea of the relative uncertainty of the cascaded gain. Keep this in mind as MMICs are cascaded.

### Noise Figure

The noise figure of a cascaded series of devices is calculated readily from the following equation.

$$NF\,(\text{total}) = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} \cdots \quad \text{(Eq 8)}$$

where noise figure (NF) and gain (G) are expressed in unitless ratios. To convert from noise figure or gain expressed in decibels to a ratio, first divide the number in dB by 10 and take the inverse base 10 log to obtain the ratio.

As an example, let's analyze the noise figure of the 2304-MHz receiving converter shown in Fig 14. Two MSA-0835 MMICs are used as RF amplifiers, followed by a band-pass filter, doubly balanced mixer and IF amplifier.

To simplify the calculation, the loss of the filter and mixer can be added to the noise figure of the IF amplifier. This allows the receiver to be analyzed as only three stages: the two MSA-0835s, each having a 4-dB NF with 13-dB gain and the filter/mixer/IF amp having a 10.5-dB NF and 10-dB gain.

$$\begin{aligned} NF\,(\text{total}) &= 2.5 + \frac{2.5 - 1}{20} + \frac{11.2 - 1}{20 \times 20} \\ &= 2.5 + 0.075 + 0.255 \\ &= 2.60 \\ &= 4.15\ \text{dB} \end{aligned}$$

This calculation assumes no additional mismatch loss. Mismatch loss can be factored in as additional loss, or as an increase in noise figure of the stage just following the mismatch.

### Compression Point

Calculating 1-dB gain compression of a series of amplifiers is not as straightforward as gain or noise figure. The 1-dB gain-compression point typically occurs several decibels after amplifier performance diverges from linearity, but it does depend on device characteristics. Unless this

(continued on page 33)

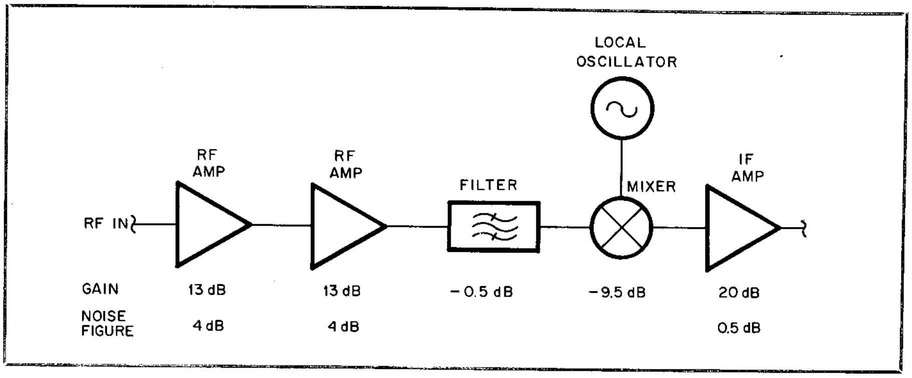



Fig 14—Block diagram of a 2.3-GHz receiving converter. To calculate the system noise figure of a cascaded series of components, the gain (or loss) and noise figure of each stage must be known.

# Monolithic Microwave Integrated Circuits

(continued from page 28)

portion of the gain curve is accurately known, it may be hard to determine which stage is actually compressing. It's also possible that two or more stages are compressing simultaneously.

The simplest solution is to ensure that the only stage driven to the 1-dB gain-compression point is the output stage. Make sure that each driver stage is running at an output power at least 3 dB, and preferably 6 dB, lower than its 1-dB gain-compression point.

**Table 3**

**Measured IMD Performance of MMIC Amplifiers**

| | *1.3 GHz* | | *2.3 GHz* | | *3.4 GHz* | |
|---|---|---|---|---|---|---|
| *Device (MSA- )* | *PEP Output (dBm)* | *3rd Order IMD Level (dB)* | *PEP Output (dBm)* | *3rd Order IMD Level (dB)* | *PEP Output (dBm)* | *3rd Order IMD Level (dB)* |
| 0485 | +12 | −32 | +12 | −28 | +12 | −28 |
| 0835 | +15 | −28 | +15 | −27 | +12 | −29 |
| 0404/0404 | +12 | −31 | +12 | −28 | Not Tested | |
| 7 × 0404 | +17 | −32 | +17 | −27 | Not Tested | |
| | +18 | −29 | Not Tested | | Not Tested | |

## IMD Products

Of great concern to amateurs who must share a band is how clean an amplifier chain will be. Undesired close-in intermodulation distortion (IMD) products must be well below the level of the fundamental signal, or the result will be "splatter" for many kilohertz on either side of the desired signal. MMICs are linear class-A devices, so they are relatively clean.

Typically when an MMIC amplifier is run up to 1-dB gain compression, the two-tone, third-order IMD products are at about 27 to 32 dB below the PEP output. For every 1-dB decrease in power output level, the third-order IMD power level will decrease by 3 dB. The IMD products relative to the desired signal decrease by $3 - 1 = 2$ dB. As power out approaches 1 dB gain compression, IMD becomes significantly worse than at lower power levels.

Measured IMD data is shown in Table 3 for several MMIC amplifiers at different frequencies. This data was taken with the amplifier power output at, or slightly greater than, the 1-dB compression point. IMD performance tends to be worse at higher frequencies.

IMD products for a cascaded series of amplifiers tend to be worse than for a single device. For example, in one test, third-order IMD products for a two-stage MSA-0404 amplifier were 2 dB worse than for a single device.