A Surface-Mount Technology Primer—*Part 1*

What makes today's compact electronics gear possible? SMT.

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The most obvious difference between traditional and surface-mount (SM) components is size. Note the relative sizes of the stamp, a conventional TO-92-case transistor on the left, and the three SM transistors on the right. Of the three SM transistors, the largest—about 4.5 × 2.5 × 1.5 mm—(in an SOT-89 package) is a general-purpose NPN silicon transistor, with a V_{CBO} of 90 V and a P_D of 1 W. The two smaller SM transistors (in SOT-23 packages) are general-purpose PNP silicon devices with a V_{CBO} of 80 V and a P_D of 200 mW.

How do manufacturers of amateur communications equipment manage to consistently offer products that provide more features, in smaller packages, with each new model? In part, this progress has been achieved through the judicious use of surface-mount devices (SMDs). SMDs provide not only significant size and weight advantages over conventional components, but are also more easily handled by automated manufacturing systems, resulting in lower manufacturing costs.

Amateurs interested in designing or maintaining their own communications equipment should know something about surface-mount technology (SMT).[1] In this article, I'll introduce you to SMT and SMDs. In Part 2, I'll discuss some of the practical aspects of working with SMDs.

Smaller, Tighter, Cheaper

Evolution in PC-board technology centers around developing different board compositions, producing thinner and more-exactly positioned traces, and minimizing production costs. The demand for denser electronic assemblies has pushed conventional PC-board technology to its limit.

Increasing circuit density by designing boards with finer and finer traces is expensive and can result in decreased reliability. Physical limits are imposed on trace width by the circuit requirements. Traces carrying power must be considerably wider than those carrying signals; a 10-mil (0.01-inch) trace can handle only about 1 A.[2] Even trace can handle only about 1 A.[2] Even the width of traces carrying only small signals cannot be reduced indefinitely. Increased path resistance—along with the crosstalk associated with more closely spaced traces—can render a circuit inoperable.

Similarly, increasing circuit density by using more circuit-board layers has practical limits. Not only do costs increase as layers are added, but board thickness and weight begin to get out of hand when more than 12 layers are used.

Surface-Mount Technology

Although SMT has received a great deal of attention lately, the surface mounting of components dates back to the hybrid assemblies of the late 1950s.[3] SMT was not fully exploited until the 1980s, however, when circuit complexity reached the point that through-hole component-mounting techniques were no longer economically or technologically feasible. Faced with the limitations of conventional PC-board technology, circuit-design engineers turned to other PC-board technologies, including SMT. SMT makes minimal use of plated-through holes and multilayer boards. In its broadest interpretation, SMT keeps components—and their interconnecting leads—on one PC-board surface, rather than feeding the component leads through the circuit board.

Modern SMT is distinguished from the surface-mount (SM) work of the 1960s and 1970s in that it involves the cost-effective methods of automated component soldering. SMT employs solder to provide electrical *and* mechanical connections between components and PC boards.[4] See Tables 1 and 2 for a summary of the benefits and limitations of SMT.

Many equipment manufacturers enter the SMT field by making mixed-technology boards—PC boards that contain SMDs and conventional devices (see Fig 1).[5] Mixed technology, or underside attachment of SMDs, has been used for almost 25 years in Japan to reduce the size and cost of electronic products.[6] This approach is also especially attractive to amateurs who would

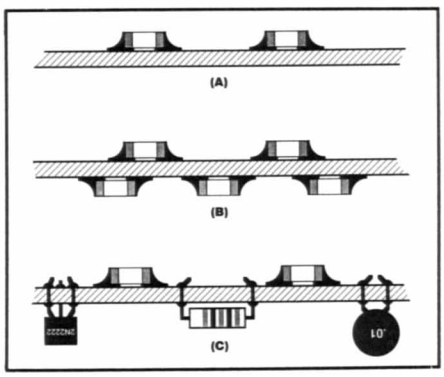


Fig 1—SMT can be used alone in single-sided board designs (A), in double-sided board layouts (B), or—more commonly—mixed with conventional leaded components (C). These so-called "mixed-technology" boards are typically populated by conventional components on one side of the board and SMDs on the other.

[1]Notes appear on p 51.

Table 1

Benefits of SMT

Of the many benefits ascribed to SMT, the most prominent include:

- Reduced component size—SMDs can be made two to five times smaller than conventional leaded components because there are no drilling tolerances to be concerned with, and no need to design components that can survive a stressful insertion process.
- Increased circuit density—pocket-size VHF transceivers, pagers and electronic watches would not be feasible without the increased density SMT affords.
- Reduced board size—smaller components and greater circuit density allow for smaller circuit boards, lowering board-material costs.
- Reduced weight—the decreased board and component size translates to lighter, more compact circuits.
- More rugged—SMD-based assemblies can be smaller, lighter and more resistant to shock and vibration than boards based on the use of conventional components.
- Less EMI—the leads of conventional components can serve as antennas that radiate and receive unwanted signals. SMDs can help minimize this problem.
- Greater interconnectivity—SMDs can be mounted with a higher number of interconnections per given area than can conventional leaded components. For example, DIPs are inefficient for components having more than 28 leads—the maximum lead count for a DIP is only 64 (the Motorola 68000, used in the Apple® Macintosh® computer is a 64-pin DIP device). By comparison, space-efficient SMDs, with *hundreds* of leads, are readily available.
- Greater reliability—as the number of board layers and interlayer connections (vias) decreases, circuit reliability increases.
- Improved high-frequency performance—the shorter interconnection paths afforded by SMDs support better high-frequency performance, in part because lead inductance and capacitance are reduced. Shorter leads and interconnections, as well as smaller package-propagation delays, also allow increased processing speeds.
- Reduced manufacturing costs—automated assembly of SMD boards and components is not only easier and less expensive, but yields are also much higher than with conventional leaded components. The pick-and-place machines used with SMDs are also less expensive than the automatic insertion machines used with conventional components.† In addition, boards designed for SMDs do not require as much drilling.
- No other options—some components are available only as SMDs, simply because their high pin count demands SM packaging.

† T. Pruce, "Make a Start with SMDs," *Electronics & Wireless World,* Dec 1989, pp 1182-1183.

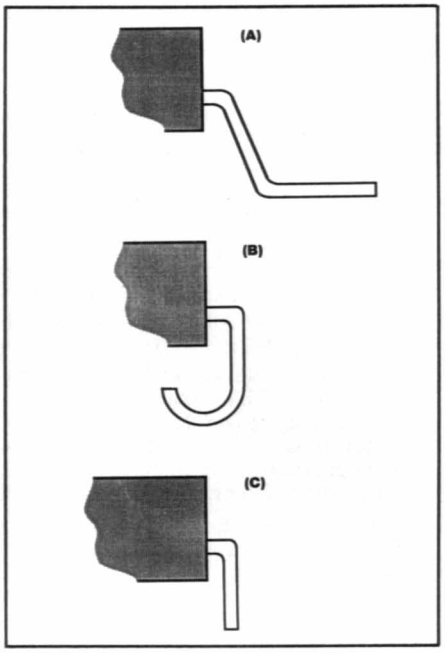


Fig 2—Popular SM lead types include gull-wing (A), J lead (B), and I lead (C). Gull-wing leads provide excellent lead access, at the cost of a considerable circuit board area requirement. Although hidden J-lead solder joints are difficult to certify visually, J leads absorb stresses due to differences in thermal coefficients of expansion and occupy less space than do gull-wing leads. I leads are more compact than either J leads or gull-wing leads, and the solder joints are easily verified visually.

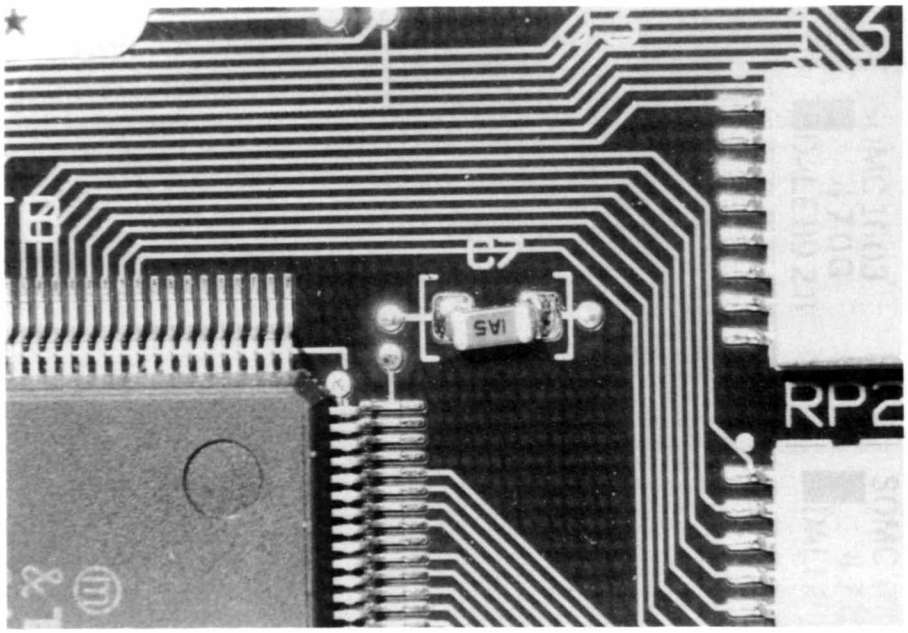


Fig 3—When troubleshooting a circuit board populated with SMDs, pay particular attention to component alignment. The alignment of the SM ceramic capacitor (C7, in the center of the photo) with its solder pad is barely within limits established for high reliability. Also shown in this photograph are sections of two 16-pin, gull-wing SM ICs (white ceramic SO packages, right) and one corner of quad flat pack IC with a few of its 196 gull-wing pins visible (black plastic package, lower left).

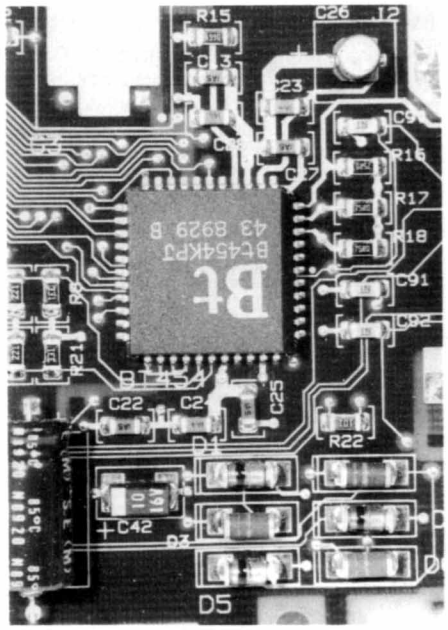


Fig 4—SMDs are available in a variety of sizes and package configurations. Note the 44-pin SM IC with I leads (center), the numerous SM resistors and ceramic capacitors (on all sides of the IC), the 10-μF tantalum capacitor (C42, lower left), and the cylindrical metal-electrode face (MELF) diodes (lower-right corner). In the lower-left corner, a conventional leaded electrolytic capacitor is also visible adjacent to C42.

Table 2

Limitations of SMT

No electronic construction technology can satisfy all circuit-design constraints. The more significant limitations of current SMT include:

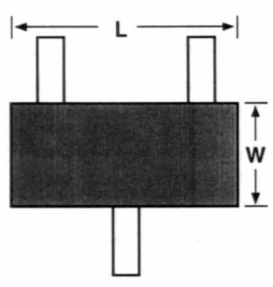
- Higher component costs. Though some SMDs cost less than their conventional counterparts, many SMDs can cost up to 50% more (in the US) because their usage volumes are currently lower. Component cost is the largest single expense in an SM assembly.†
- Lack of component availability. High-power (greater than 1-W) diodes, precision (1% or better) resistors, some digital ICs, and capacitors rated at more than a few hundred microfarads are currently hard to source. This situation is expected to improve in the near future, as the industry moves to 100%-SM assemblies.
- Evolving packaging standards. With the exception of passive devices, relatively little standardization of SM packaging has been achieved.‡ Whereas there are only about a dozen different, well-established DIPs to choose from, there are over 120 different SM packages in use.†† Since each manufacturer may produce a given component in a different package, second-sourcing becomes difficult, if not impossible. In general, a given circuit must be designed with a specific SMD supplier in mind.
- Retooling costs. Because one machine or one technique cannot be used with all SMDs, costs for conversion from conventional components to SMDs can be prohibitive for some manufacturers. For the amateur, additional expenses can be incurred as well—for visual aids, fine-tipped, temperature-controlled soldering irons, precision tweezers, etc.
- Poor heat dissipation. The higher component density made possible by SMT translates to more heat per unit area, which must be dissipated in order to avoid premature component failure. In addition, the SMD's smaller leads make heat conduction away from components more difficult. That is, SMD packages tend to exhibit higher thermal resistance than conventional packages. More-efficient devices and more-aggressive cooling techniques, including forced-air cooling, must be employed with some SM assemblies. In some cases, the demand for SM versions of particular components, eg, SM power diodes, cannot be met until packaging capable of greater dissipation is developed.‡‡
- Thermal mismatch. SMDs and the PC boards they are mounted on typically have markedly different coefficients of thermal expansion (the coefficient of thermal expansion for a ceramic component is less than half of that of an organic PC board), which can result in board warping and fracturing with normal thermal cycling. New circuit-board substrates and SM packages are being developed to minimize this problem.
- Difficult testing. The poor node visibility and tight lead spacing associated with some SM packages make manual testing difficult. Visual aids, microtip probes, and a steady hand are mandatory for testing SM assemblies.
- Decreased mechanical strength. The solder-only connections associated with SMDs are less robust than the conventional through-the-board mounting. Because the difference in expansion of the components and the PC board (over a board's operating-temperature range) must be entirely absorbed by these solder joints, soldering must be performed with much greater care than with conventional components.
- New learning curve. Working with SMDs requires an understanding of how to best match components and PC-board substrates, how the layout of PC-board pads and traces affect performance, and how to work with new soldering techniques and tools.

†S. McClelland, "What is Surface Mount Technology?" *Advancing Surface Mount Technology: An IFS Executive Briefing,* ed. S. McClelland (New York: Springer Verlag, 1988), pp 3-5.

‡B. Richards, "The Sensitivity of Surface Mount Technology to Component Quality," *Advancing Surface Mount Technology: An IFS Executive Briefing,* S. McClelland ed., (New York: Springer Verlag, 1988), pp 143-154.

††P. McCormic, "Integrated Circuit Design for Surface Mount Technology," *Advancing Surface Mount Technology: An IFS Executive Briefing,* S. McClelland ed., (New York: Springer Verlag, 1988), pp 29-34.

‡‡A. Turner, "SMT—Dream or Reality," *Electronics & Wireless World,* Dec 1989, p 1179.



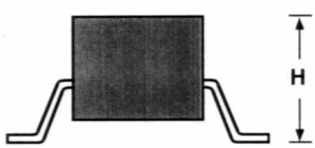


Fig 5—The SOT-23 package outline. Nominal package dimensions are approximately 3.0 (L) × 1.5 (W) × 1.0 mm (H).

like to gradually work SMT into their repertoire of construction options.

Surface-Mount Devices

A number of SMT packaging alternatives have been developed, each for a particular class of applications.[7] The packaging used for active SMDs (transistors and ICs) tends to be quite different from that used for resistors, capacitors and other passive SMDs.

Active-Device Packaging

The most common SMD packaging alternatives available for multiple-lead, active devices include small outline (SO), quad flat pack (QFP), plastic-leaded chip carrier (PLCC), tape-automated bonding (TAB), and leadless ceramic chip carrier (LCCC) packaging. In addition to variations in the SMD body, packaging alternatives include component-lead configuration. The three lead configurations most commonly used with SM packages are the gull-wing, **J**-lead, and **I**-lead (see Fig 2).

The gull-wing lead (used on the large ICs shown in Fig 3) flares out and downward from the device body. Virtually all SO IC packages employ gull-wing leads. While lending itself to easy visual inspection and probing, the gull-wing design is susceptible to lead damage during handling and its footprint is relatively large.

The **J** lead (Fig 2B) is protected against damage because the lead is rolled under the package. The **J**-lead configuration provides higher mounting densities at the expense of reduced manufacturing yields,[8] difficulty in examining solder connections and increased package height.

The **I** lead (used on the large IC in Fig 4) provides most of the advantages of the **J** lead, including greater possible mounting densities, but requires that the leads be tinned prior to use.

Of the SM IC packages, the SO configuration, developed by Philips in 1971 for the watch industry, is the oldest. It also remains the most common mounting package for SM ICs with up to 28 pins (see Fig 3).

The QFP package, designed to handle devices with 64 to 196 pins, uses gull-wing leads to achieve extremely close lead spacing (see Fig 3).

PLCC packages were developed for components with up to 84 pins, using **J**-lead pins on all four sides to minimize mounting area and for ease of handling.

LCCC packages rely on metallized pads on the underside of the chip, instead of leads, for soldering to PC boards. Although the LCCC is the ultimate SM package in terms of compactness, touch-up and repair are virtually impossible, because of the many blind, uninspectable solder areas that bond an LCCC device to its board. In addition, because there are no leads to absorb the stresses of thermal expansion, LCCC components must be mounted on special substrate materials, such as copper-clad Invar, which have

coefficients of thermal expansion near that of the ceramic component body. As a benefit, the heat dissipation qualities of an LCCC/Invar board combination are excellent.

SM transistors are most commonly available in molded plastic SO packages, with gull-wing leads that can be directly mounted on the PC board. The particular small-outline-transistor (SOT) packaging used for a given component is generally a function of the device's lead count and power-dissipation requirements. For example, the three-terminal SOT-23 package (see Fig 5 and the title-page photo), is generally used for small-signal transistors and diodes capable of dissipating up to 200 mW. In comparison, the larger three-terminal SOT-89 package (see the title-page photo) is used for devices requiring power dissipations up to 500 mW.

Next Month

In Part 2, I'll discuss passive-device packaging and how to work with SMDs, and will provide a list of SM device and tool suppliers.

Notes

[1]For those who'd like a hands-on approach to learning more about SMT, Heathkit® offers a surface-mount technology course (EI-3135) for $99.95. Contact Heath Co, PO Box 8589, Benton Harbor, MI 49022-8589, tel 800-253-0570.

[2]C. Simon, *Computer Aided Design of Printed Circuits*, 1987 (San Francisco: Abbot, Foster & Hauserman Co, 1987), pp 1-12.

[3]These hybrid units, built for their small size and improved high-frequency performance, were constructed by interconnecting chip resistors, capacitors, and bare semiconductor dies on rigid ceramic substrates. Similarly, the IC flatpack, commonly used in the 1960s, predated the popular dual inline package (DIP). See R. Clark, *Planning the Printed Circuit Manufacturing Environment*, (New York: Van Nostrand Reinhold, 1989), p 178.

[4]Contrast this with hybrid circuit design, in which components are first mechanically attached to a ceramic or other rigid substrate with adhesives, and the components are then electically connected to pads on the substrate using fine gold wires.

[5]B. Morris, "SMD Reworking," *Electronics & Wireless World*," Dec 1989, pp 1176-1178.

[6]T. Takei, "Soldering Techniques for Manufacturing Surface Mount Devices," *Advancing Surface Mount Technology: An IFS Executive Briefing*, S. McClelland ed., (New York: Springer Verlag, 1988), pp 95-102.

[7]Although this situation has improved in the past few years with the formalization of standards, at least between American and European semiconductor manufacturers, it is not uncommon to see component package types referenced to standards proposed by the IPC (Institute for Interconnecting and Packaging Electronic Circuits), JEDEC (Joint Electronic Device Engineering Council), EIA (Electronics Industries Association), and the EIAJ (Electronics Industries Association of Japan)—all in the same components catalog.

[8]S. Hinch, *Handbook of Surface Mount Technology* (Essex, England: Longman Scientific & Technical, 1988).